11 Black-Jack Dealer

11.1 Specification

A Black-Jack dealer is a device which plays the dealer's hand of a card game. Its inputs are *go* (true/false) and *card* (Ace of Spades,...,2 of clubs). Its outputs are *hitme*, *stand*, and *broke* (all truth-valued).

The *go*/*hitme* signals are used for a 4-cycle handshake with the operator. Cards are valued from 2 to 10, and aces may be valued as either 1 or 11 by choice of the player. The Black-Jack dealer is repeatedly presented with cards. It must assert *stand* when its accumulated score reaches 16; and it must assert *broke* when its score exceeds 21. In either case the next card starts a new game.

A design specification of the Black-Jack dealer can be found in the text book "The Art of Digital Design" by D. Winkel and F. Prosser [WiPr80].

11.2 Implementation

The implementation of the black jack dealer has been taken from [WiPr80]. From the abstract description of an FSM controlling the datapath, the following realization has been derived (Fig. 11-1). The FSM has been realized by encoding the states with two flipflops A and B and generating the next state by choosing the right signal with two 4:1 multiplexers (table 11-1).

State	Next State	B	A	Condition
0 Get	Get	0	0	nGet_2
	Add	0	1	Get_2
1 Add	Use	1	0	Acecard & nAce11flag
	Test	1	1	not(Acecard & nAce11flag)
2 Use	Test	1	1	true
3 Test	Get	0	0	nTest_3
	Test	1	1	Test_3

Table 11-1: State transition table

The flipflop output signals are fed to a combinational logic to generate the controller output signals as described in the equations from table 11-2 and table 11-3.:

Get_1	=	S_Get & nCard_r_s
Get_2	=	S_Get & Card_r_s & nCard_r_d
Get_3	=	Get_2 & (Stand v Broke)
Test_1	=	S_Test & ScoreGT16 & nScoreGT21
Test_2	=	S_Test & ScoreGT16 & ScoreGT21 & nAce11flag = S_Test & ScoreGT21 & nAce11flag
Test_3	=	S_Test & ScoreGT16 & ScoreGT21 & Ace11flag = S_Test & ScoreGT21 & Ace11flag

Table 11-2: Internal signals

Hit	=	Get_1
Set_Stand	=	Test_1
Clr_Stand	=	Get_2
Set_Broke	=	Test_2
Clr_Broke	=	Get_2

Table 11-3: Output signals

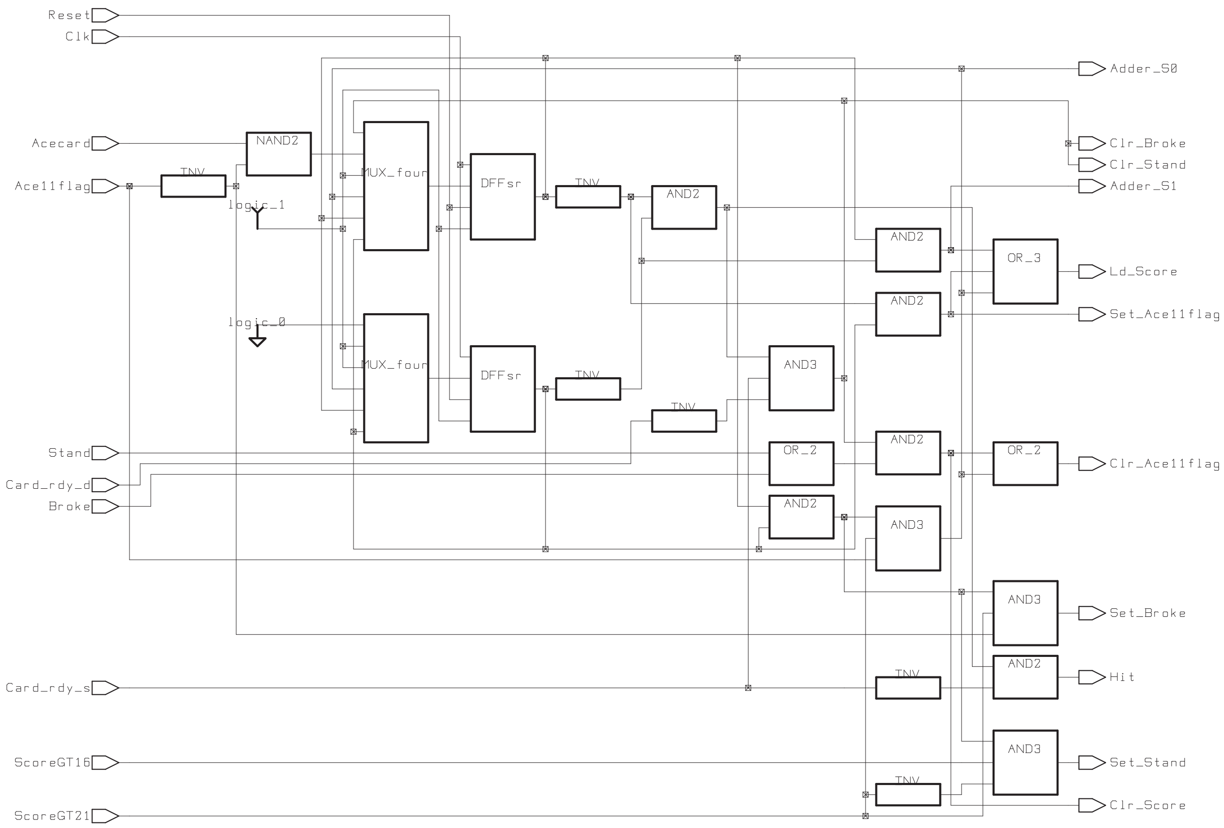

Figure 11-1: Controller of the Black-Jack Dealer

Set_Ace11flag	=	S_Use
Clr_Ace11flag	=	Get_3 v Test_3
Ld_Score	=	S_Add v S_Use v Test_3
Clr_Score	=	Get_3
AdderS0	=	S_Add
AdderS1	=	Test_3

Table 11-3: Output signals

The second part of the dealer is BlackJack_DataPath (Fig. 11-2), including several flipflops to hold the status information for the outside world, hit, stand, broke, to debounce the input signal from a card ready button and to hold the ace11flag. The circuit uses the card_value input signal to discriminate the value of an ace card from others, indicating this by setting the signal ace-card = true. card_value is then expanded by one bit and fed to a 4:1 multiplexer, which has to choose between D'+10', D'-10' and the actual card value according to table 11-4.

Mux input	AdderS1	AdderS0	action
0	0	0	+10
1	0	1	-10
2	1	0	value
3	1	1	-

Table 11-4: Data path function

The multiplexer is followed by a 5-bit carry ripple adder, adding the actual score internal_score and the output of the multiplexer. The sum internal_sum is then fed to a 5-bit register with load and clear, which is controlled by the signals Ld_Score and Clr_Score, to produce the score.

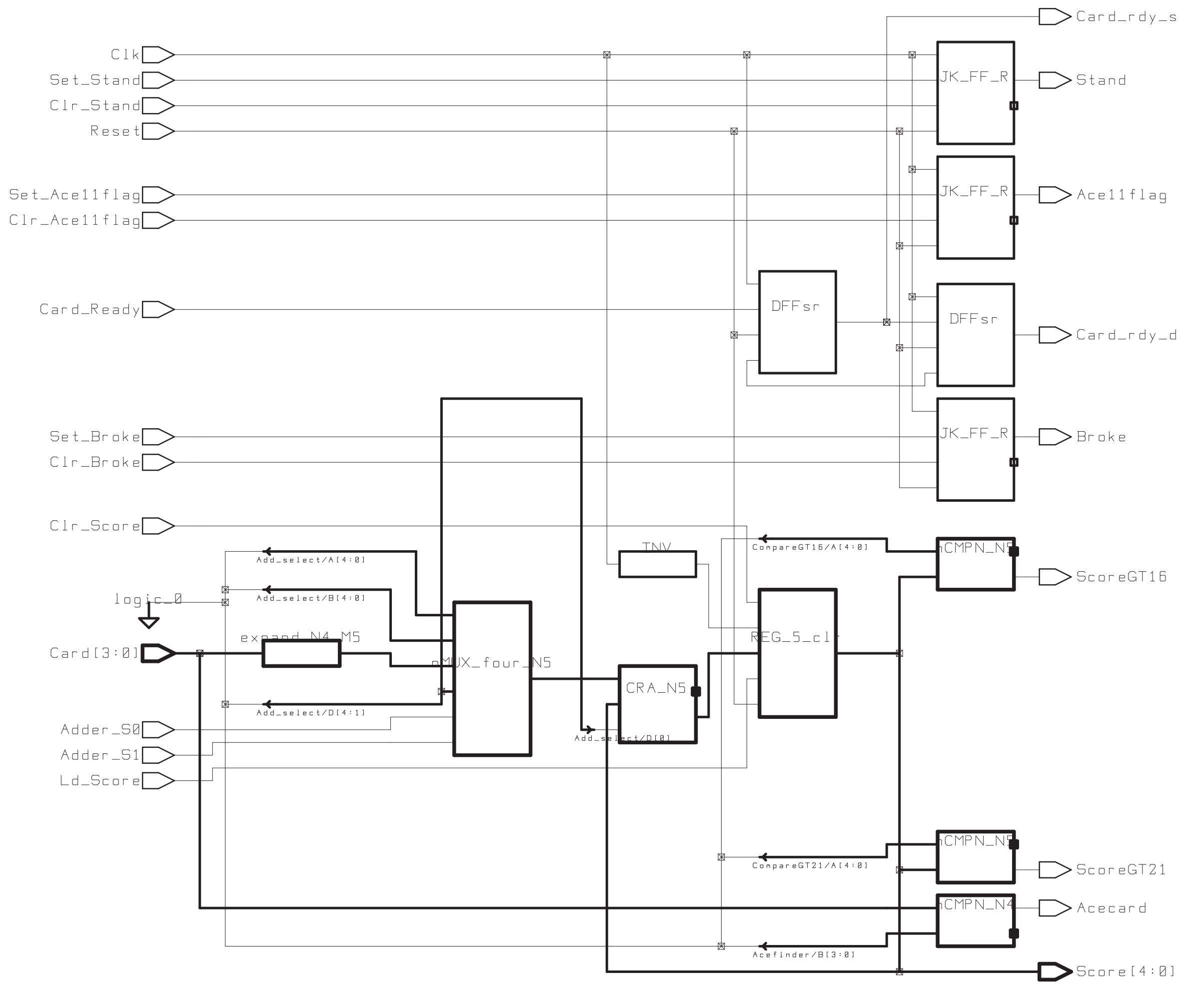

Figure 11-2: Datapath

The score is then compared with D'16' and D'21' to generate the signals ScoreGT16 and ScoreGT21. Both units exchange control signals as viewed in Fig. 11-3.

The waveform diagram in Fig. 11-4 shows the exchange of control signals between the units. The signals test(0) to test(3) contain the state signals S_Get, S_Use, S_Add, S_Test. The signal test_dp(4:0) contains the internal sum before it is taken over by the register.

The waveform diagram in Fig. 11-5 shows the behavior of the black jack dealer as a black box. Moreover, the behavior of a algorithmical VHDL description has been added.

11.3 Status and Acknowledgments

Thanks for C.-J. Thomas for providing an implementation description.

The circuit has been originally proposed by J. Staunstrup. Most of the specification has been directly quoted from [Stau93].

11.4 Literature

[WiPr80] D. Winkel and F. Prosser. *The Art of Digital Design*. Prentice-Hall Inc., 1980.

[Stau93] J. Staunstrup. IFIP WG 10.2 collection of circuit verification examples, November 1993.

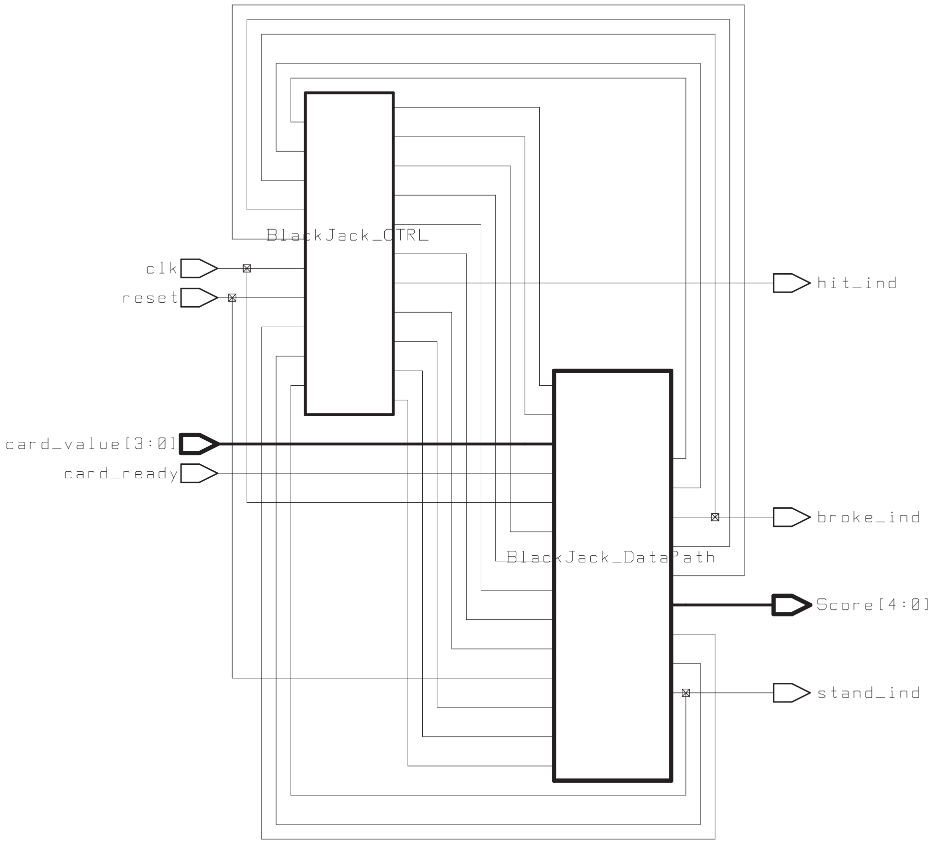

Figure 11-3: Control - data path communication

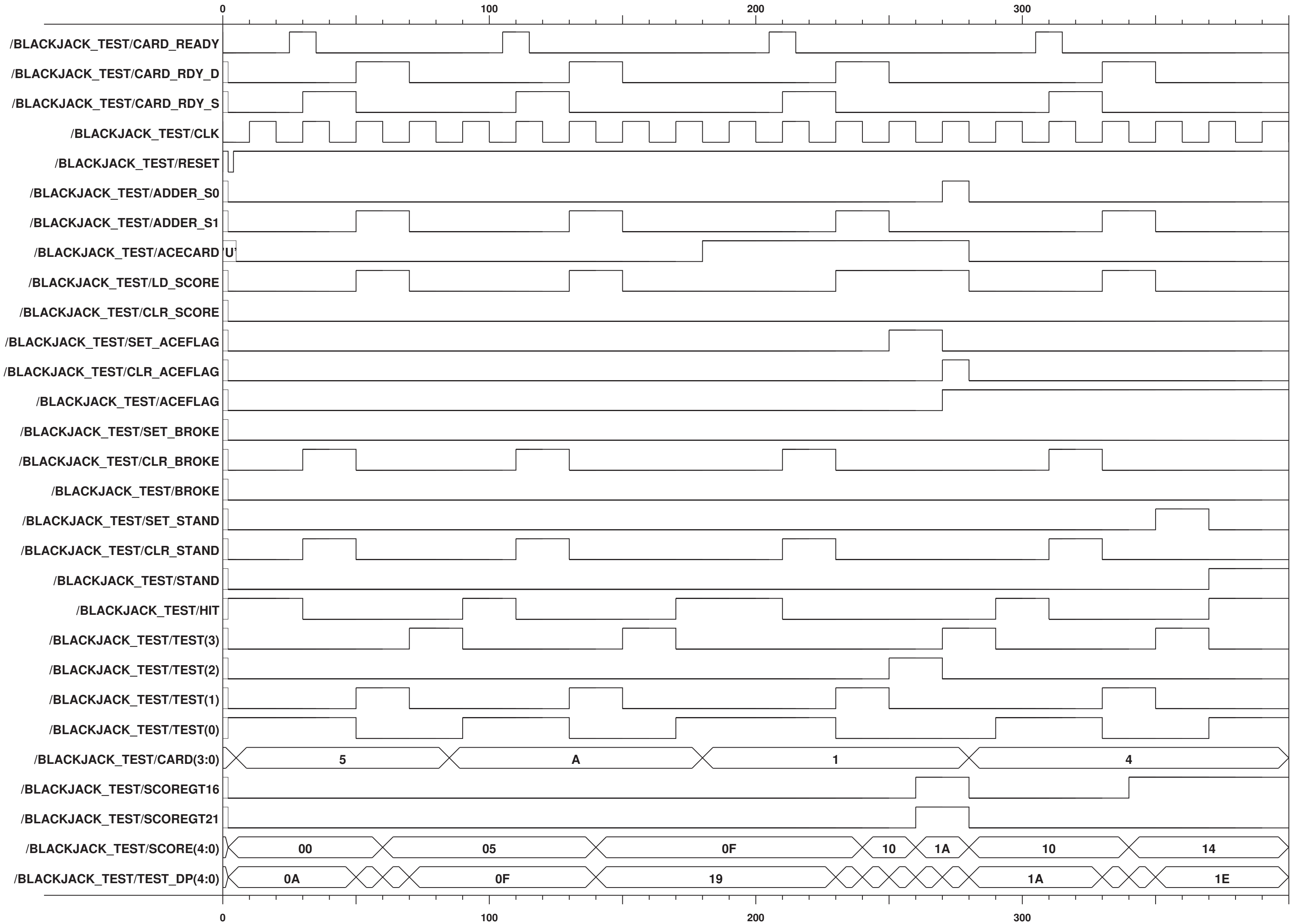

Figure 11-4: Waveform diagram of internal signals

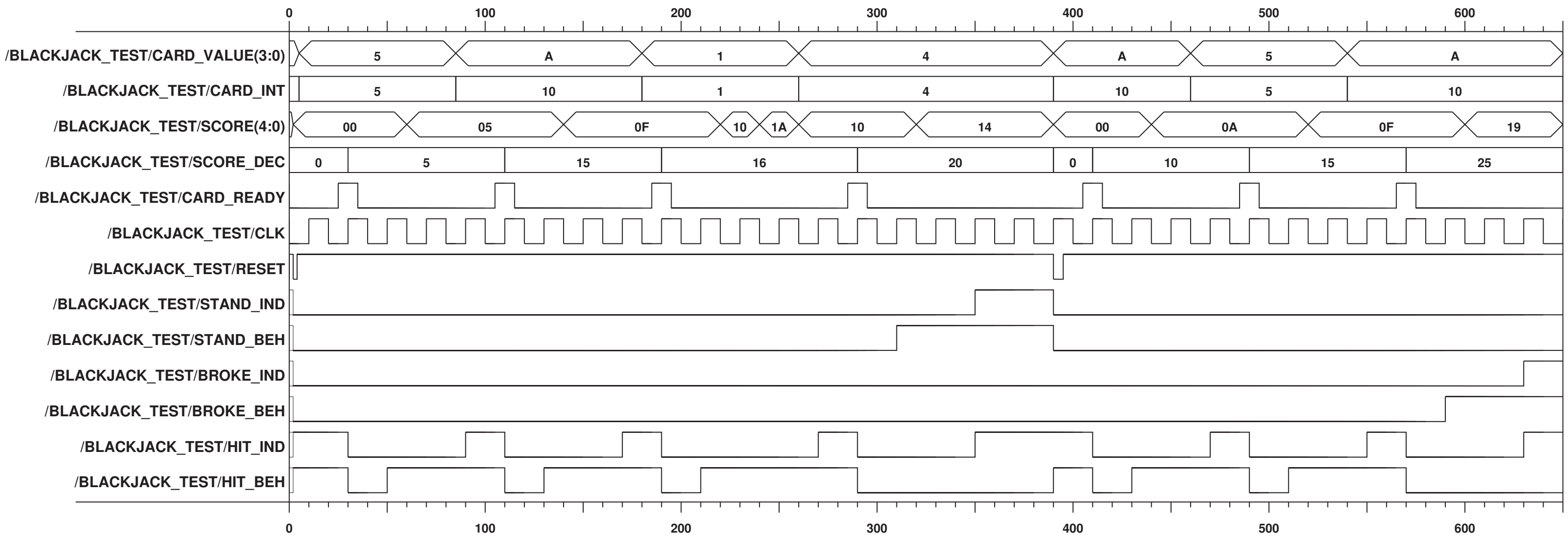

Figure 11-5: Blackbox simulation of the circuit