**Question 1**

a)

FPGA’s have several advantages some are:

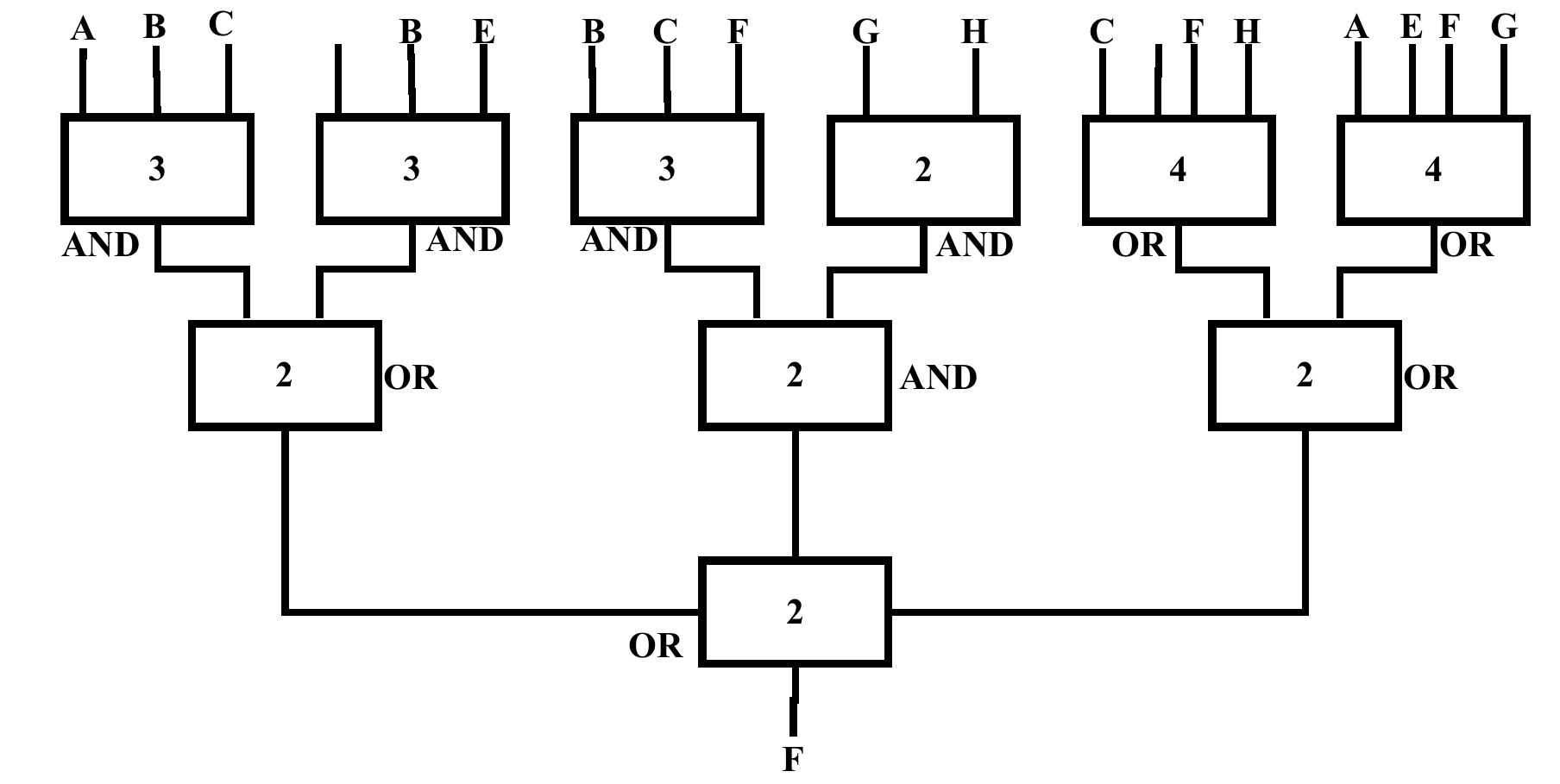
1. Ease of prototyping
2. Fast prototyping
3. Low cost of prototyping
4. Re-programmability
5. Availability of variety of FPGAs with embedded units
6. Availability and friendliness of tools
7. Fast testing of the circuit

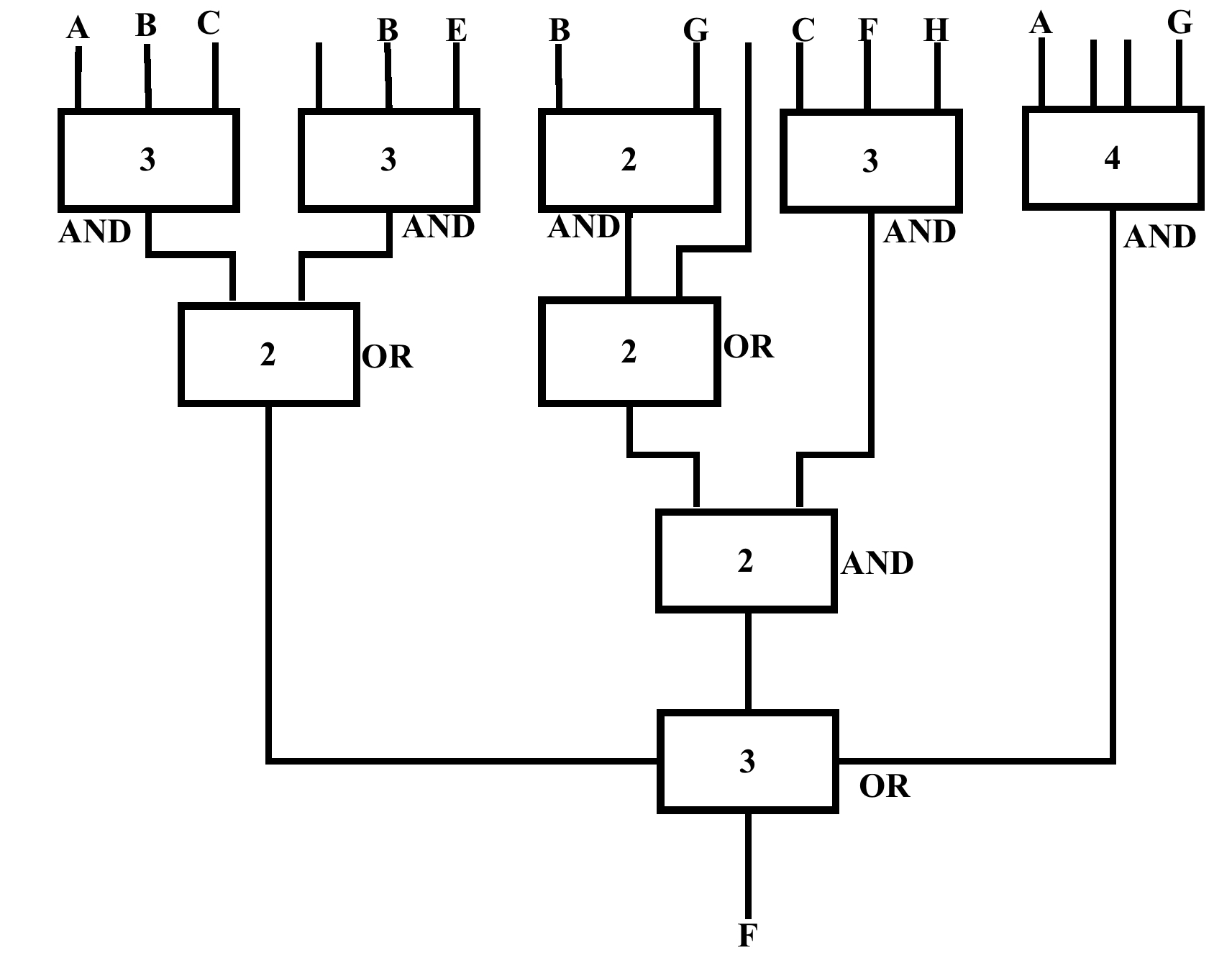
b)

F(A,B,C,D,E,F,G,H) =

F can be implemented with a variety of 2,3 and 4 variable LUT. In here, we give 2 implementations selected due to their lowest delay.

|  |  |  |
| --- | --- | --- |
| Delay |  | Area |
| 4 |  |  |
| 2 |  |  |
| 3 |  |  |
| 9 |  | 124 |





|  |  |  |
| --- | --- | --- |
| Delay |  | Area |
| 2 |  |  |
| 2 |  |  |
| 2 |  |  |
| 3 |  |  |
| 9 |  | 98 |

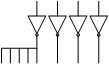
The second implementation has the same delay, but the better area.

**Question 2**

Z is inverted and it is added to one get its –ve value and NOT XORed since we want is –ve.

1+

extension ….



+1

|  |  |  |  |  |  |  |  |  |  |
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|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  | 1 |  |

Critical Path

H

H

H

+

H

H

+

+

+

+

+

+

+

+

+

+

+

+

+

+

+

H

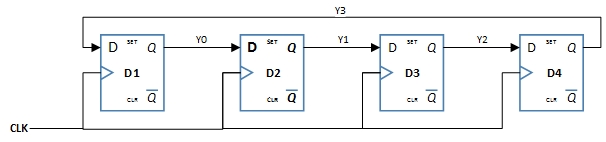
1

**Question 3**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | | | | Next State | | | |  |  |
|  |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |  |  |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |  |  |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |  |  |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |  |  |



From the table above:



|  |  |  |
| --- | --- | --- |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | 00 | 01 | 11 | 10 |
| 00 |  | 1 | X |  |
| 01 |  | X | X |  |
| 11 |  | X | X |  |
| 10 |  | X | X |  |

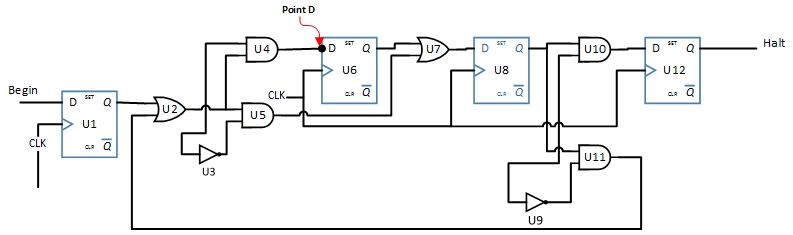
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | 00 | 01 | 11 | 10 |
| 00 |  |  |  |  |
| 01 |  |  |  |  |
| 11 | X | X | X | X |
| 10 | 1 | X | X | X |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | 00 | 01 | 11 | 10 |
| 00 |  |  |  |  |
| 01 | 1 | X | X | X |
| 11 | X | X | X | X |
| 10 |  |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | 00 | 01 | 11 | 10 |
| 00 |  |  | X | 1 |
| 01 |  |  | X | X |
| 11 |  |  | X | X |
| 10 |  |  | X | X |

**Question 4**

a)



There are 6 paths:

Path1:

Path2:

Path3:

Path4:

Path5:

Path6:

b)

Path delay at point D, which is path 5.

at point D, is

is path 1 delay, , ,

c)

When clock skew is introduced between and the rest. We calculate the changes to the path. Path 4 is the longest path.

New critical path has been introduced. This is the added delay at the input of since CLK of other FFs is taken as a reference.

**Question 5**

a)

Typical Delays

@ Ambient temp of 27

Delay Variations

, 0.909 voltage variation

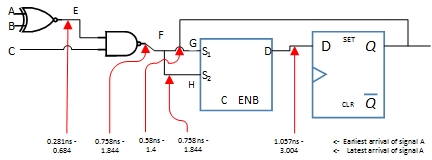
Junction Temp Variation

De-rating Temp Variation

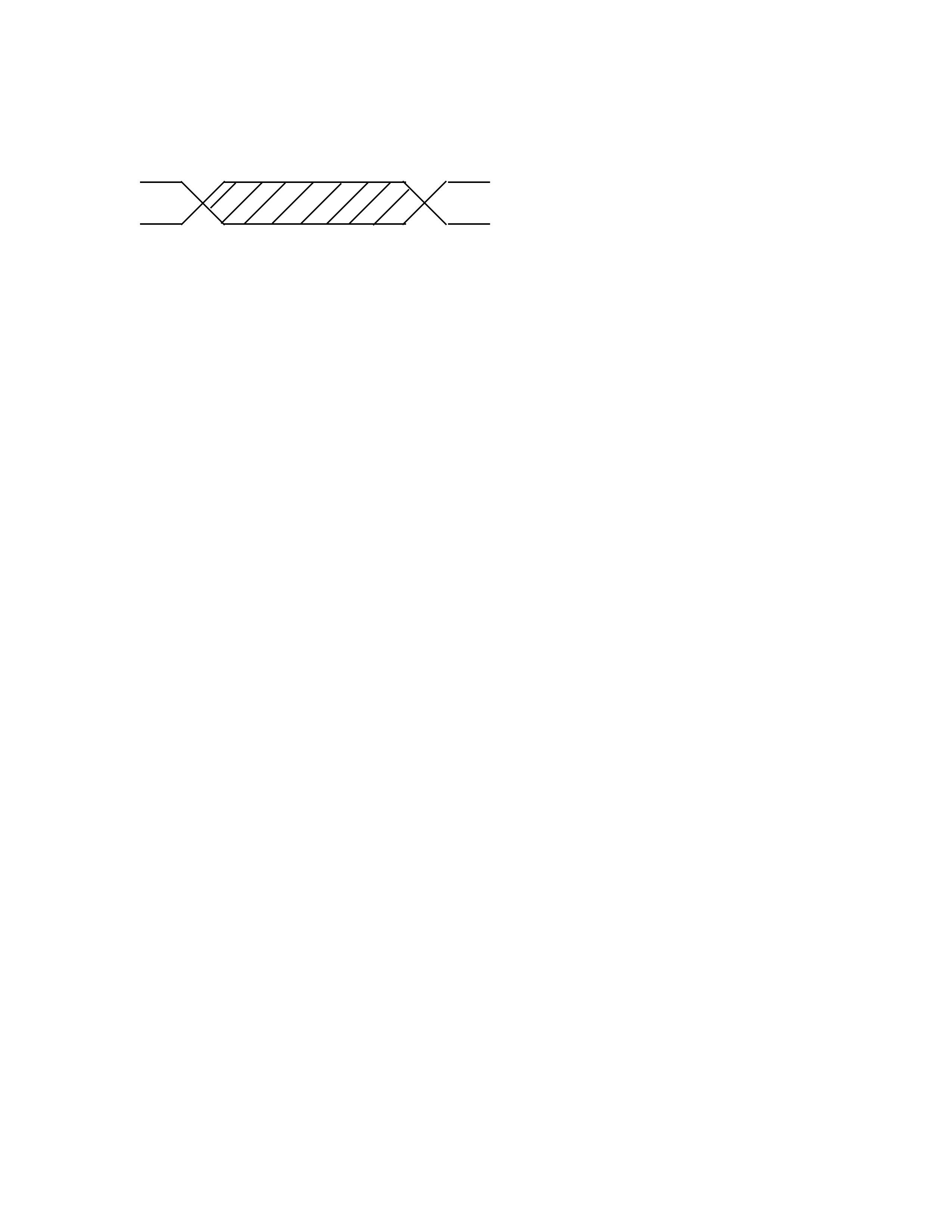
Composite De-rating factor

Min/Max delay

Min, Max Delay of the Gates used in Figure 2



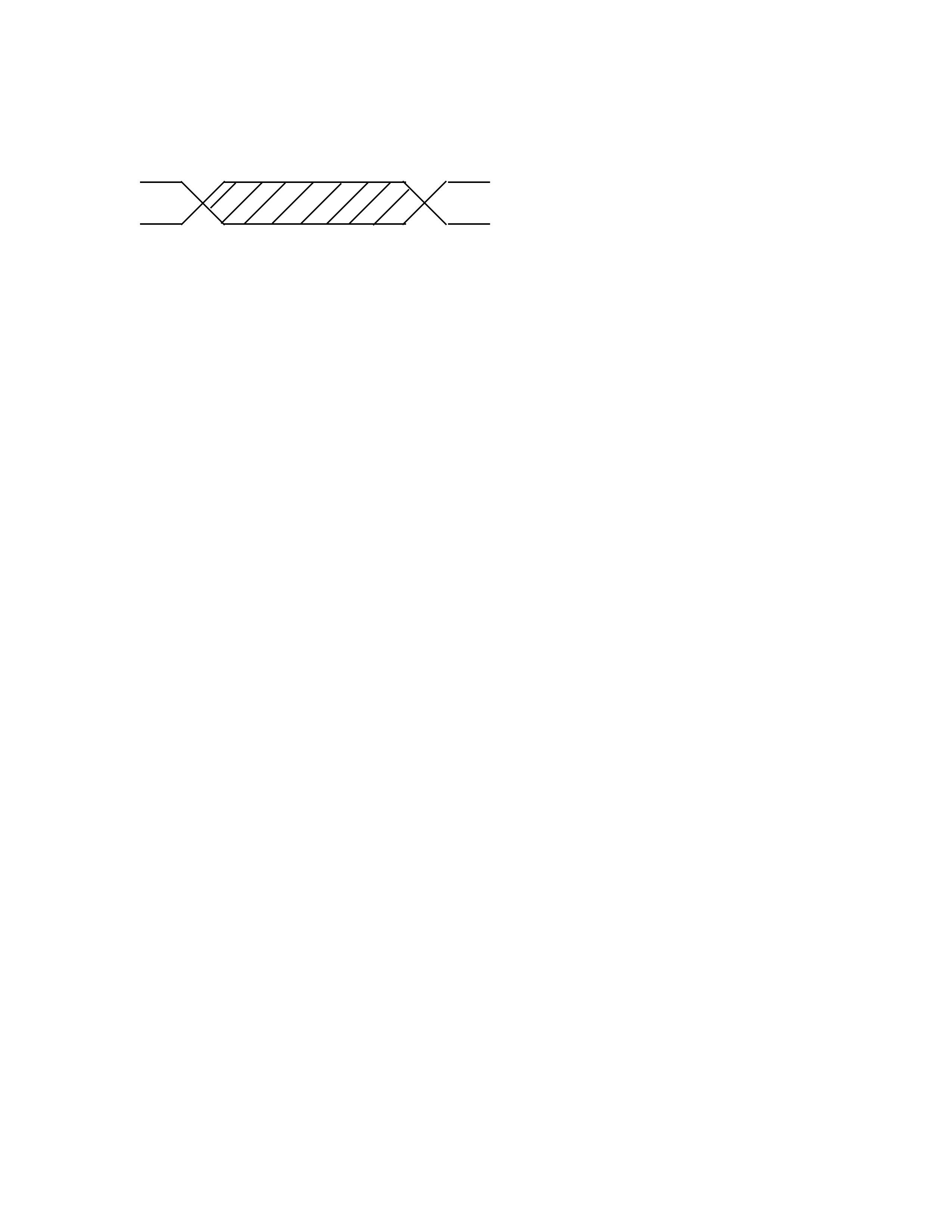
D-input



Latest arrival

3.004

1.057



b)

Total Period

**Question 6**

a)

There are many ways of writing this piece of code. Here is just a simple example:

library IEEE;

use IEEE.std\_logic\_1164.all;

entity exam\_circuit is

port (A, B : in std\_logic;

O1,O2 : out std\_logic);

end exam\_circuit

architecture structural of exam\_circuit is

component decoder2to4

port(a, b : in std\_logic;

d1, d2, d3, d4 : out std\_logic);

end component decoder2to4;

component AND\_gate

port(in1, in2 : in std\_logic;

out1 : out std\_logic);

end component AND\_gate;

component OR\_gate

port(in1, in2 : in std\_logic;

out1 : out std\_logic);

end component OR\_gate;

signal d1, d2, d3, d4 : std\_logic;

begin

decoder1: decoder2to4 portmap (A, B, d1, d2, d3, d4);

AND1 : AND\_gate portmap (d1, d2, O1);

OR1 : OR\_gate portmap (d3,d4, O2);

End structural

b)

L2: X,Y : I std\_logic

L4: end Half\_A\_Con

L5: H\_A\_Behav

L7: -signal

L8: process(X,Y)

L13: problem of conversion X,Y

L17: endif