ABB HAFO
INTEGRATED CIRCUIT
RAD-HARD TECHNOLOGY

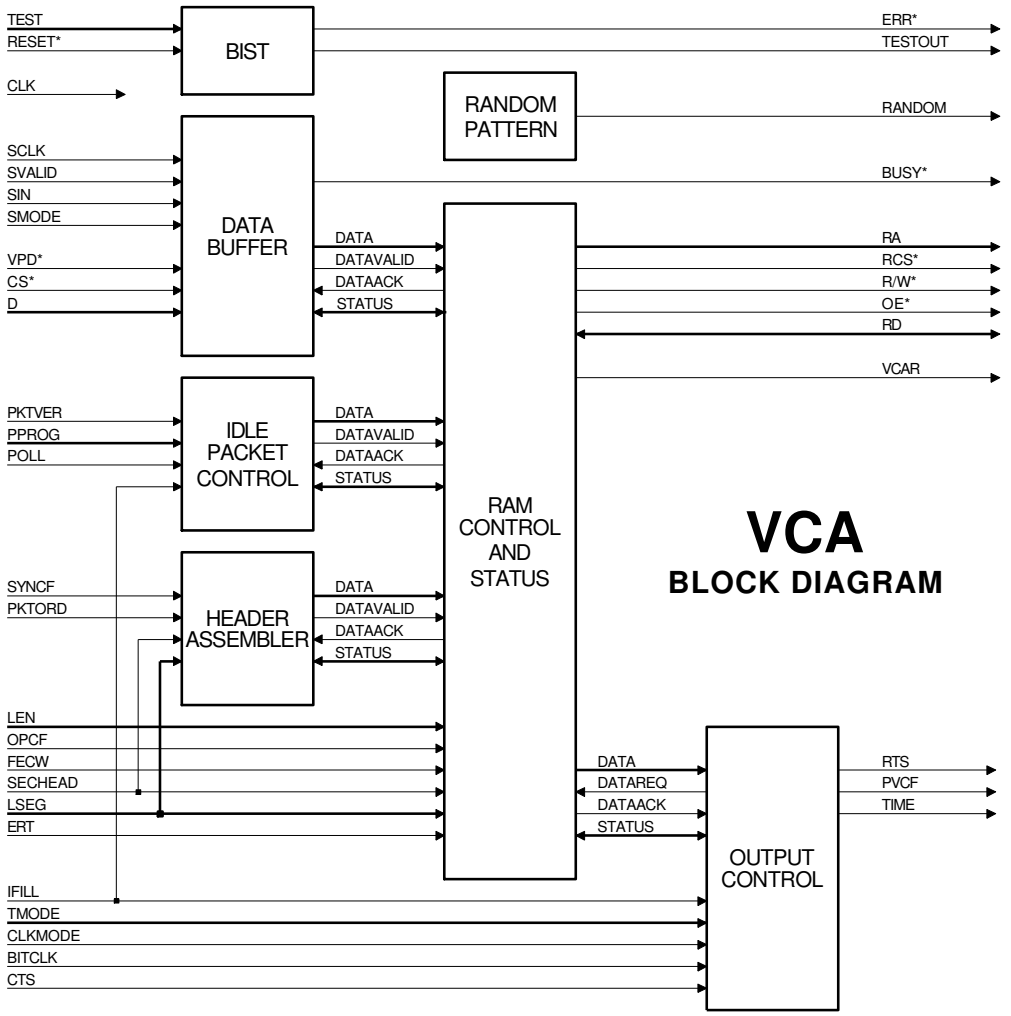
VCA HAF_12399
VIRTUAL CHANNEL ASSEMBLER
PRELIMINARY DATA SHEET January, 1994

Description

The Virtual Channel Assembler (VCA) generates parts of Packet Telemetry Transfer Frames. One Virtual Channel Multiplexer (VCM) together with one VCA per Virtual Channel, up to a maximum of eight, form a complete Transfer Frame Generator.

The VCA receives data from the on-board data handling system, in parallel or serial form, and stores them in an external 8k x 8 RAM buffer. When requested to deliver a partial Transfer Frame to the VCM, the VCA generates parts of the header and outputs the data from the RAM. If no data are available a partial Idle Transfer Frame is output.

To ensure that Telemetry Packets in an incomplete Transfer Frame can be made available to the VCM, the VCA itself can generate and insert Idle Telemetry Packets.



VCA
BLOCK DIAGRAM

Features

- Fully compliant with CCSDS and ESA Packet Telemetry Standard
- Selectable frame length 223, 446, 892 or 1115 octets, with full support for the First Header Pointer
- Generates strobe for time sampling
- CMOS/SOS technology; radiation hard, latch-up free, very low SEU sensitivity
- ESA/SCC part number 9544/005, to be qualified in Q2 1994
- Built-In Self Test (BIST)
- Up to 12.5 MBit/s operation

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Table of Contents

1	INTRODUCTION	3
1.1	Reference documents	3
1.2	System overview	3
2	TRANSFER FRAME AND IDLE TELEMETRY PACKET FORMATS	6
2.1	Transfer Frame format	6
2.2	Partial Virtual Channel Frame format	6
2.3	Idle Telemetry Packet format	8
3	FUNCTIONAL SPECIFICATION	10
3.1	Summary of operation	10
3.2	Functions not included in the VCA	10
3.3	Parallel input interface	10
3.4	Serial input interface	12
3.5	Storage of data in external RAM	14
3.6	Virtual Channel Frame Counter	16
3.7	First Header Pointer	17
3.8	VCA/VCM interface	18
3.9	Idle Transfer Frames	18
3.10	Idle Telemetry Packet insertion	20
3.11	Pseudo-random Idle Fill data	22
3.12	Time sampling strobe	22
3.13	Test	23
3.14	State after reset	23
4	INTERFACE AND SIGNAL DESCRIPTION	24
4.1	Parallel input interface, 12 pins	25
4.2	Serial input interface, 4 pins	26
4.3	RAM interface, 24 pins	27
4.4	VCM interface, 5 pins	28
4.5	Time sampling strobe, 1 pin	28
4.6	Operational mode selection, 18 pins	29
4.7	Miscellaneous, 20 pins	31
5	ELECTRICAL AND MECHANICAL DATA	33
5.1	Absolute maximum ratings	33
5.2	DC specifications	33
5.3	AC specifications	35
5.4	Mechanical data	40
6	ABBREVIATIONS	42

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1 INTRODUCTION

1.1 Reference documents

RD1 Packet Telemetry Standard, ESA PSS-04-106 Issue 1
RD2 VCM Data Sheet, ABB HAFO

1.2 System overview

The Virtual Channel Frame Assembler (VCA) device is a part of the VCA/VCM chip set supporting the ESA Packet Telemetry Standard RD1. The VCA receives Telemetry Packets from an OBDH system, or non-packet data from instruments, tape recorders etc., and stores them in an external RAM of standard type. Upon request, the VCA assembles a partial Transfer Frame, which is sent to the Virtual Channel Multiplexer (VCM) described in RD2. The VCA operates at a maximum clock frequency of 12.5 MHz, resulting in a maximum peak bit rate of 12.5 Mbit/s.

The VCA supports Transfer Frame lengths of 223, 446, 892 or 1115 octets, each with four different trailer options. The Transfer Frame length and trailer type are selected by four input pins instead of using a mode register, which would have been SEU sensitive.

One VCM together with one to eight VCAs are used to generate Packet Telemetry Transfer Frames. Each of the VCAs can assemble partial Transfer Frames, which are multiplexed and completed by the VCM. One VCA device and one 8k x 8 RAM are required per Virtual Channel. A typical environment for the VCA is shown in figure 1.

The VCA receives data from a source in the form of octets, using either a parallel or a serial input interface. In the latter case, data are assembled into octets, which are internally forwarded to the parallel interface. The VCA can accept any type of data structure, not only Telemetry Packets. For Transfer Frame bit rates lower than 3 Mbit/s, the VCA can use a clock with higher frequency than the bit clock, allowing an input data rate independent from the bit rate used. For higher bit rates, the VCA and VCM should use the same clock, and the maximum input data rate is double the bit rate.

The partial Transfer Frame generated by the VCA consists of three octets of the Transfer Frame Header, optionally including a Secondary Header, and the Transfer Frame Data Field with the input data. The VCA fully supports the First Header Pointer, and has therefore no requirement on aligning the packets with the Transfer Frame boundary.

The VCM built-in selection algorithms determine which of the VCAs are ready to send a non-idle partial Transfer Frame by observing their Ready To Send (RTS) signals. When a partial Transfer Frame shall be output, the VCM asserts the corresponding Clear To Send (CTS) signal. If the VCA has stored enough data for at least one complete Transfer Frame, the VCA first outputs the three octets of the Transfer Frame Header, optionally outputs the Secondary Header, then outputs the Transfer Frame Data Field, starting with the data first transferred to the VCA from the data source.

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If the VCA is requested to output a partial Transfer Frame, but an insufficient amount of data is available, it will generate and output a partial Idle Transfer Frame, resulting in an Idle Transfer Frame being output from the VCM, to ensure correct operation of the ground equipment. Any Virtual Channel can be used to generate Idle Transfer Frames, regardless of whether it is used for sending Telemetry Packets as well. However, the VCM built-in selection algorithms use the VCA associated to Virtual Channel 7 for Idle Transfer Frames.

The VCM receives the partial Transfer Frame from the selected VCA, adds the first three octets of the Virtual Channel Header, and optionally generates the Trailer, thus forming a complete Transfer Frame.

The VCA asserts a strobe that can be used to read out the spacecraft on-board time, to be sent to the ground in a Telemetry Packet. The strobe interval is programmable for all intervals defined in the Packet Telemetry Standard RD1.

The VCA can optionally generate and insert Idle Telemetry Packets, to fill up an incomplete Transfer Frame. This feature can be used to ensure that the last packets in a VCA will be sent to the ground, even if no subsequent data are input, for example in the case when an instrument has been switched off. The Idle Telemetry Packet insertion is started when a built-in counter has reached a preprogrammed number of polls from the VCM, without the VCA having enough data for a non-idle Transfer Frame. This feature is only available when the VCA is operating with Telemetry Packets.

The VCA operating mode is determined by input pins. The VCA features Built-In Self Test (BIST), that can be automatically activated after reset.

Note: the VCA is designed to be used on the same circuit board as the VCM and a Reed-Solomon encoder, forming a Transfer Frame Generator.

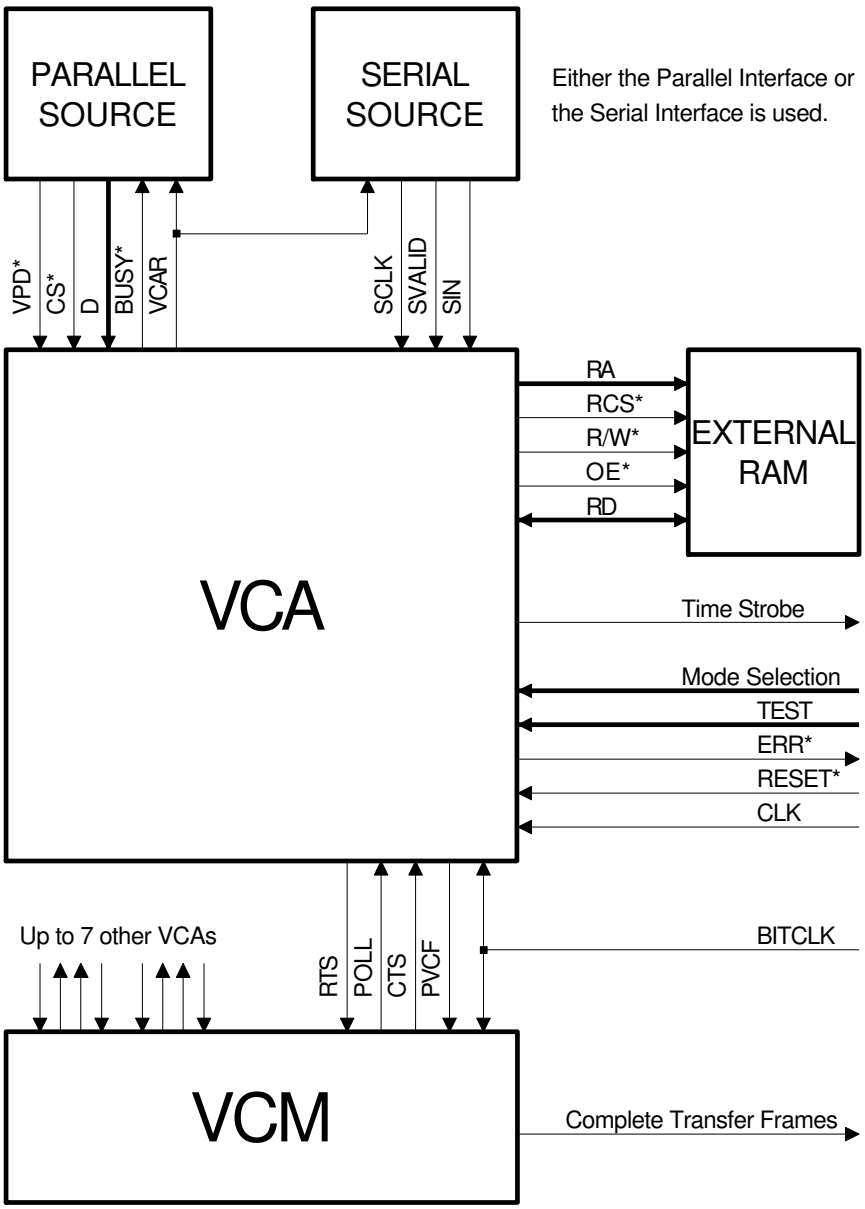

Figure 1: Typical application environment for the VCA, both a serial and a parallel source is shown, though only one of the interfaces can be used at a time

2 TRANSFER FRAME AND IDLE TELEMETRY PACKET FORMATS

In section 2.1 the Transfer Frame format is described. In section 2.2 the Partial Virtual Channel Frame fields are described and the different Transfer Frame and Partial Virtual Channel Frame lengths are specified. In section 2.3 the format of the Idle Telemetry Packets is described.

Throughout this document bit 0 is the most significant bit and is input/output first when transferred as a serial bit stream.

2.1 Transfer Frame format

A Transfer Frame is composed of a Primary Header, an optional Secondary Header, a Data Field and an optional Trailer and has the following structure:

<table>
<tr><td colspan="5">Transfer Frame</td></tr>
<tr><td>By VCM</td><td colspan="3">Partial Virtual Channel Frame, by VCA</td><td>By VCM</td></tr>
<tr><td colspan="2">Transfer Frame Header</td><td colspan="2">Transfer Frame Data Field</td><td rowspan="2">Transfer Frame Trailer (optional)</td></tr>
<tr><td colspan="2">Primary</td><td>Secondary (optional)</td><td>ket | Packet | Packet | Packet | Pa</td></tr>
<tr><td>3 oct.</td><td>3 oct.</td><td>0/4 octets</td><td></td><td>0/2/4/6 octets</td></tr>
<tr><td colspan="5">223/446/982/1115 octets</td></tr>
</table>

The VCA and VCM can generate Transfer Frames of four possible lengths: 223, 446, 892 and 1115 octets. This selection allows a span of Transfer Frame lengths that are usable both with and without Reed-Solomon encoding.

2.2 Partial Virtual Channel Frame format

The Partial Virtual Channel Frame (PVCF) is a result of the split of the functionality between the VCA and the VCM. The PVCF is only an internal structure, not defined in the Packet Telemetry Standard, and can be disregarded from the system point of view. Often the expression partial Transfer Frame can be used interchangeably with PVCF.

A PVCF is composed of the last three octets of the Transfer Frame Primary Header, the optional Secondary Header and the Data Field.

The VCM adds a Synchronisation Marker, the first three octets of the Primary Header and an optional Trailer to the PVCF to produce a complete Transfer Frame. The number of octets inserted into the Transfer Frame Data Field by the VCA depends on the values of the four static inputs as defined in table 1 and whether a Secondary Header is present.

The size of the PVCF depends on both the length of the Transfer Frame defined by the LEN0 and LEN1 inputs, and whether the Operational Control Field (OPCF) and/or the Frame Error Correction Word (FECW) will be generated by the VCM, as determined by the OPCF and FECW inputs. The PVCF lengths are:

Transfer Frame length	LEN0	LEN1	OPCF	FECW	PVCF length
223 octets	0	0	0	0	220 octets
223 octets	0	0	0	1	218 octets
223 octets	0	0	1	0	216 octets
223 octets	0	0	1	1	214 octets
446 octets	0	1	0	0	443 octets
446 octets	0	1	0	1	441 octets
446 octets	0	1	1	0	439 octets
446 octets	0	1	1	1	437 octets
892 octets	1	0	0	0	889 octets
892 octets	1	0	0	1	887 octets
892 octets	1	0	1	0	885 octets
892 octets	1	0	1	1	883 octets
1115 octets	1	1	0	0	1112 octets
1115 octets	1	1	0	1	1110 octets
1115 octets	1	1	1	0	1108 octets
1115 octets	1	1	1	1	1106 octets

Table 1: PVCF Length

The structure of the PVCF Header as generated by the VCA is:

Part of Transfer Frame Primary Header (always present)						Transfer Frame Secondary Header (optional)		
Virtual Channel Frame Count	Frame Data Field Status					Secondary Header ID		Sec. Header Data
	Sec. Header Flag	Sync Flag	Packet Order Flag	Segment Length ID	First Header Pointer	Secondary Header Version No.	Sec. Header Length	
8 bits 0...7	1 bit 0	1 bit 1	1 bit 2	2 bits 3...4	11 bits 5...15	2 bits 0...1	6 bits 2...7	24 bits 0...23
1 octet	2 octets					0/4 octets		

The contents of the PVCF Header fields are:

Field Contents	
Virtual Channel Frame Count:	
Virtual Channel Frame Count (bit 0 to 7):	8 LSBs of the Virtual Channel Frame Counter
Frame Data Field Status:	
Secondary Header Flag (bit 0)	SECHEAD input pin
Data Field Synchronisation Flag (bit 1):	SYNCF input pin
Packet Order Flag (bit 2):	PKTORD input pin
Segmentation Length Identifier (bit 3 to 4):	LSEG0 and LSEG1 input pins
First Header Pointer (bit 5 to 15):	As described in section 3.7
Secondary Header: [1]	
Secondary Header Version Number (bit 0 to 1):	00
Secondary Header Length (bit 2 to 7):	000011
Secondary Header Data (bit 0 to 23):	24 MSBs of the Virtual Channel Frame Counter

1) The Transfer Frame Secondary Header is optional: its presence or absence is indicated by the Secondary Header Flag within the Primary Header.

2.3 Idle Telemetry Packet format

The VCA can optionally insert Idle Telemetry Packets into an incompletely filled Transfer Frame, in order to fill it so it can be sent to the ground.

The Idle Telemetry Packet comprises a Packet Header with a length of six octets and a Data Field with a fixed length of eight octets, giving a total Idle Telemetry Packet length of 14 octets. The Idle Telemetry Packets have been kept short, in the case a Telemetry Packet should arrive during the Idle Telemetry Packet insertion process.

The structure of this Idle Telemetry Packet is:

Idle Telemetry Packet Header							Idle Telemetry Packet Data Field
Packet Identification				Packet Sequence Control		Packet Length	
Version Number	Type	Data Field Header Flag	Appli-cation Process ID	Segment-ation Flags	Source Sequence Count		
3 Bits 0...2	1 bit 3	1 bit 4	11 bits 5...15	2 bits 0...1	14 bits 2...15	16 bits 0...15	64 bits 0...63
2 octets				2 octets		2 octets	8 octets

The VCA generates the Idle Telemetry Packet according to:

Field Contents	
Packet Identification:	
Version Number MSB (bit 0):	Value of PKTVER input pin [1]
Version Number LSBs (bit 1 to 2):	00
Type (bit 3):	0
Data Field Header Flag (bit 4):	0
Application Process Identifier (bit 5 to 15):	11111111111
Packet Sequence Control:	
Segmentation Flags (bit 0 to 1):	11
Source Sequence Count (bit 2 to 15):	00000000000000
Packet Length:	
Packet Length (bit 0 to 15):	0000000000000111 [2]
Idle Telemetry Packet Data Field:	
Idle Telemetry Packet Data Field (bit 0 to 63):	Data from IFILL input pin [3]

1) The PKTVER input pin allows the version number for the Idle Telemetry Packet to be selected; when PKTVER = 0 version 1 packets are generated (Packet Version field = 000), when PKTVER = 1 version 2 packets are generated (Packet Version field = 100).

2) The value 7 corresponds to (Idle Telemetry Packet Data Field length) - 1.

3) Normally connected to the RANDOM output pin.

3 FUNCTIONAL SPECIFICATION

3.1 Summary of operation

After reset and the optional self-test, the VCA provides the following functions:

- Reception of data from the OBDH system, which are stored in an external RAM together with header data.
- When requested by the VCM, a partial Transfer Frame is output, consisting of the PVCF Header, optionally including a Secondary Header, and the Transfer Frame Data Field.
- If enough data are not available an partial Idle Transfer Frame is output instead.
- Optional generation of Idle Telemetry Packets to fill up incomplete Transfer Frames.
- Generation of Pseudo-random Idle Fill data, used for the generation of partial Idle Telemetry Packets and Idle Transfer Frames.
- Generation of a Time sampling strobe.

In order to complete the Transfer Frame the VCM performs the following functions:

- Generation of the 32 bit Synchronisation Marker.
- Generation of the first three octets of the Transfer Frame Primary Header.
- Feed-through of the PVCF data as part of the Transfer Frame.
- Generation of an optional Transfer Frame Trailer.
- Optionally leaving space for a Reed-Solomon code check block.

3.2 Functions not included in the VCA

The VCA does not perform segmentation of Source Packets, which should be done by the data source. The VCA can handle Telemetry Packets and data blocks longer than 8k octets, though only a part of the data will reside in the external RAM at a time.

The VCA does not check the contents or the format of the Telemetry Packets provided by the source. Thus the VCA is independent of the Telemetry Packet format and any data structure can be used. The only exception is the Idle Telemetry Packets that optionally can be generated by the VCA itself, which have a predefined structure.

3.3 Parallel input interface

The parallel interface, shown in figure 2, is active when SMODE = 0. The serial interface inputs SCLK, SVALID and SIN are then disabled but should be held to a defined logic level.

The main functions of the parallel input interface are:

- To latch data from the input bus and into the VCA.
- To inform the data source that the VCA has space in the external RAM.
- To detect the beginning of Telemetry Packets or data blocks being sent from the source and to set the First Header Pointer accordingly.

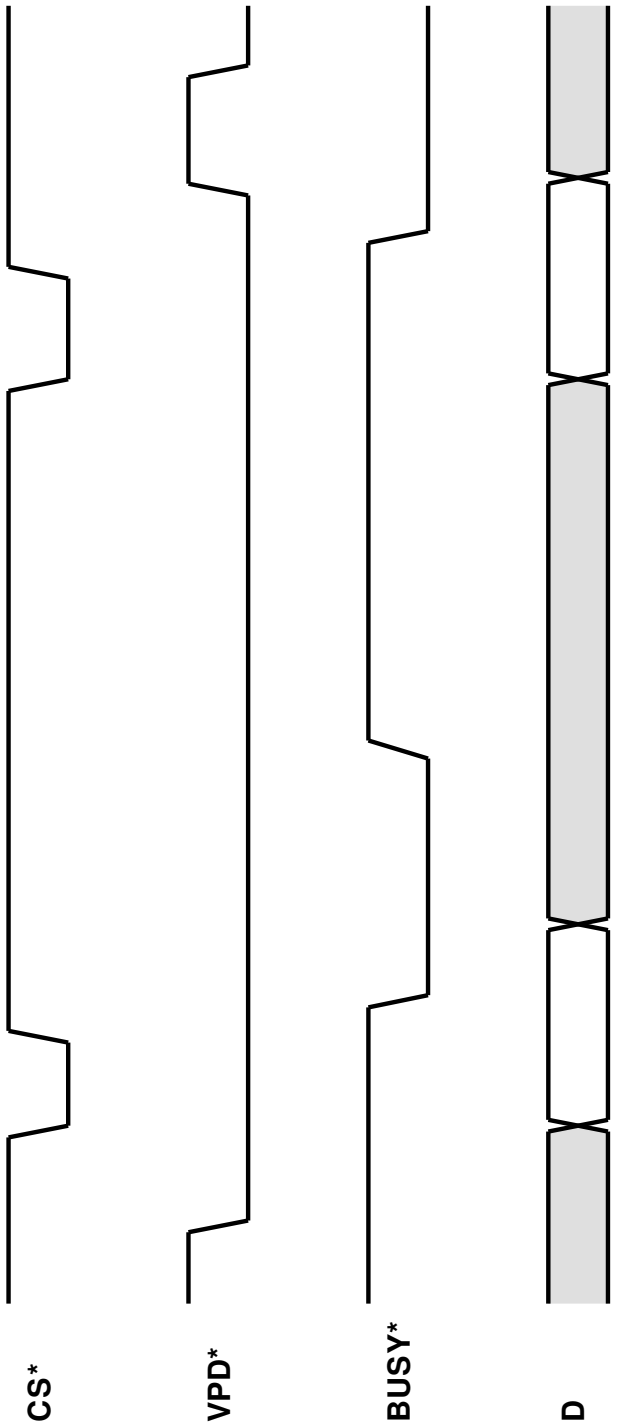

Figure 2: Parallel input interface

Data are input from the data source using the eight-bit wide data bus (D0 - D7), and the chip select, CS*. The interface is asynchronous. Data are latched into the VCA on the rising CS* edge, as shown in figure 2. Note: D0 is the MSB.

The active low Valid Packet Data (VPD*) input defines when a new Telemetry Packet (data block in **asynchronous** mode) starts. The VCA stores data latched by the input interface when the VPD* input is asserted (VPD* = 0). The VPD* input should be continuously asserted while a Telemetry Packet is being input. The timing of VPD* is shown in figure 2. VPD* is also used to set the First Header Pointer, as described in section 3.7.

Data may be supplied at any rate up to one octet transfer every four CLK cycles, allowing a maximum peak input data rate of 25 MBit/s when operating at the maximum clock frequency of 12.5 MHz. If data are input at a higher rate, data could be lost.

In the case of using Telemetry Packets with a limited length (LSEG ≠ 11) the VCA Ready (VCAR) output is asserted when there is room for at least one maximum-length Telemetry Packet in the external RAM. Otherwise the VCAR output is asserted when there is room for at least one Transfer Frame Data Field. The threshold for VCAR being asserted is defined in section 4.1.4.

Since VCAR is asserted when there is room for a predefined amount of data (one maximum-length Telemetry Packet alternatively one Transfer Frame Data Field), this data can be transferred in its entirety without needing to check VCAR again.

The BUSY* (VCA Busy) output is asserted (BUSY* = 0) immediately after an octet has been written into the VCA (i.e. the rising CS* edge). BUSY* is de-asserted at the next falling CLK edge three CLK cycles after the rising CS* edge. Since CS* may be asynchronous, the actual duration of BUSY* asserted can vary between three and four CLK cycles. BUSY* is also asserted when there is no space for more octets in the external RAM. If CS* is asserted while BUSY* is asserted no data will be latched.

The VCAR output alone can be used together with data sources that provide data with a transfer rate which is less than the maximum possible, while the BUSY* output can be used with fast data sources that need acknowledge on the octet level, such as a CPU.

3.4 Serial input interface

The serial input interface, shown in figure 3, is enabled when SMODE = 1. The parallel interface inputs CS*, VPD* and D0 - D7 are disabled, but should be held to a defined logic level. The VCAR and BUSY* outputs and all other functions of the VCA behave the same as for the parallel input interface, though they are probably less useful for the serial interface.

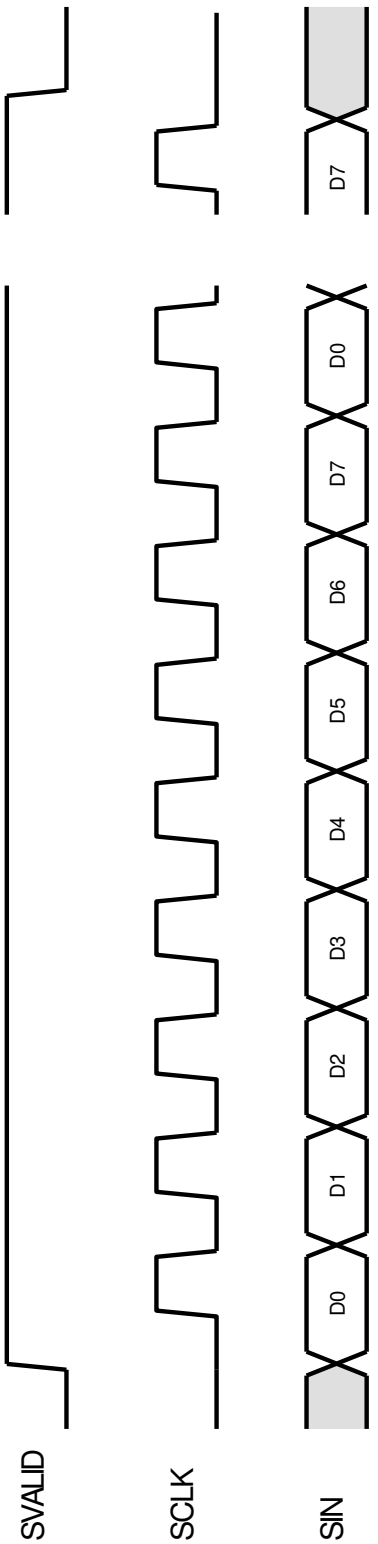

Figure 3: Serial input interface

Serial data are clocked in on the rising SCLK edge, when SVALID = 1. The serial data are assembled in a shift register and when eight bits have been input, the resulting octet is internally forwarded to the parallel interface. Data should consist of multiples of eight bits otherwise the last bits will be lost.

The input signal SVALID is used to delimit Telemetry Packets (data blocks in **asynchronous** mode), in the same way as VPD* is used for the parallel interface. It shall be asserted while a Telemetry Packet (data block) is being input. In addition, SVALID defines the octet boundaries in the input data stream, the first octet explicitly and the following octets each subsequent eight SCLK cycles; the first bit received after SVALID has been asserted is bit 0. SVALID shall be asserted when data are input.

SCLK is asynchronous and need thus not be correlated to the CLK, except for the maximum input data transfer rate (one octet per four CLK cycles).

3.5 Storage of data in external RAM

The VCA interfaces to an external 8k x 8 static RAM to store PVCF data until the VCM requests them. The VCA RAM interface is shown in figure 4. The interface timing ensures that no bus collisions occur due to the VCA and RAM driving output data at the same time, also for consecutive read and write cycles. The VCA can be used with RAMs such as MA9264 from GEC Plessey Semiconductors and HM65664 from Matra MHS, among others.

The VCA is capable of storing a variable number of PVCFs, ranging from 7 of the maximum length PVCFs to 36 of minimum length. Table 2 shows the relationship between the Transfer Frame length and the maximum number of PVCFs that can be stored.

Transfer Frame length	Maximum number of PVCFs that can be stored
223	36
446	18
892	9
1115	7

Table 2: Transfer Frame length versus maximum number of PVCFs stored

The VCA generates the RAM address (RA0 - RA12), the Chip Select (RCS*), the Read/Write strobe (R/W*) and the Output Enable (OE*). Data are transferred to and from the RAM over the bidirectional data bus (RD0 - RD7.) The duration of the read and write cycles generated by the VCA are two CLK cycles. When the VCA does not access the RAM the RD data bus is still driven to ensure that the bus is not left floating.

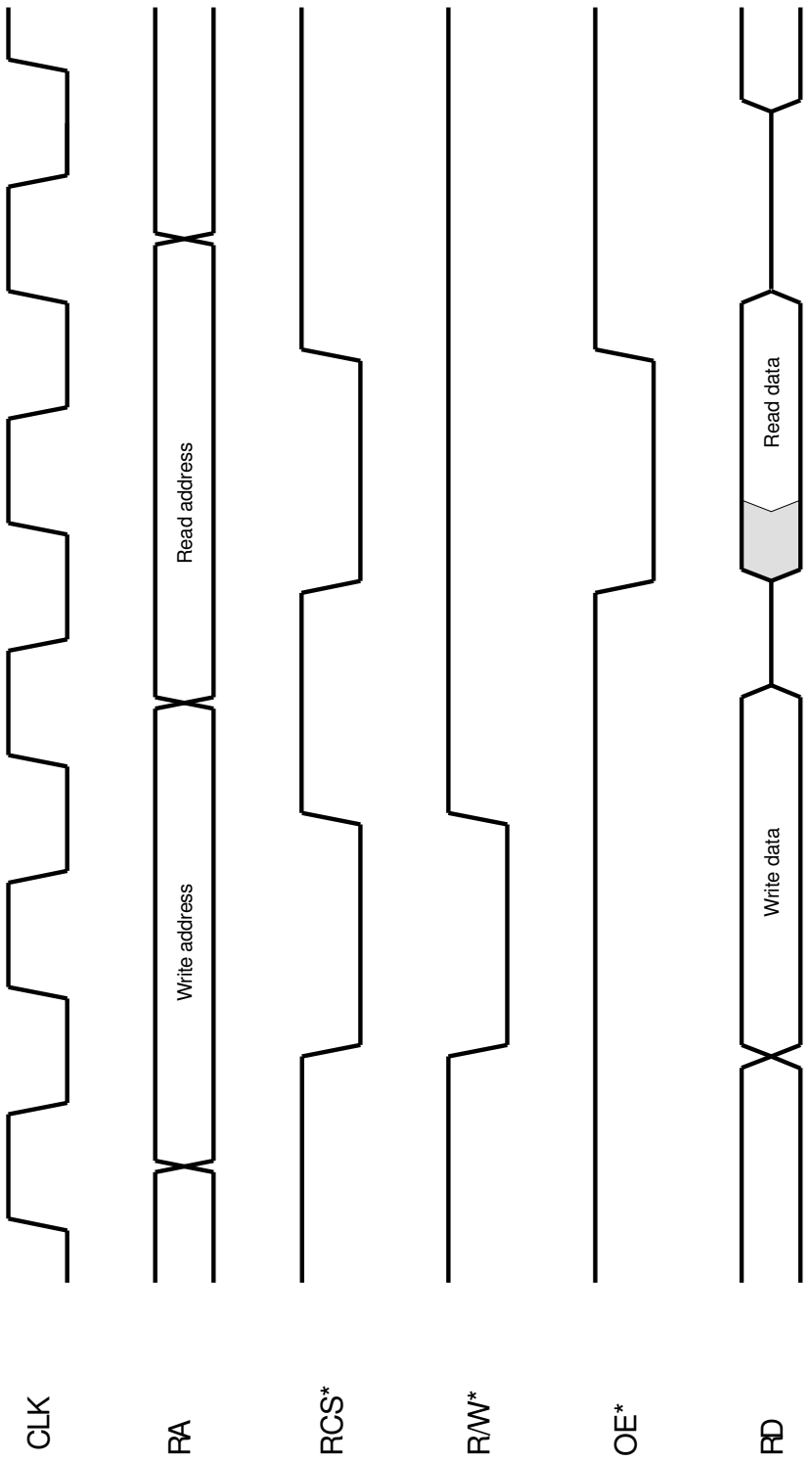

Figure 4: RAM interface timing

Once a PVCF transfer to the VCM has started, the VCA continues to output the PVCF data without interruption. Therefore during the output of a PVCF to the VCM, the VCA reads PVCF data from the RAM once every eight CLK cycles (BITCLK cycles, when CLKMODE = 1).

The maximum input data rate is one octet every four CLK cycles, and thus the VCA may be required to write input data to the RAM once every four CLK cycles. In addition, Transfer Frame Header data and Idle Telemetry Packets are written to the RAM without disturbing the above RAM accesses.

3.6 Virtual Channel Frame Counter

To verify that all Virtual Channel Frames have been received and in the correct order, the VCA has a 32 bit wrap-around Virtual Channel Frame Counter, which is incremented for each PVCF, normal and idle.

The VCA assigns the eight LSBs of the Virtual Channel Frame Counter to the Virtual Channel Frame Count field in the Primary Header. When the Secondary Header is present (SECHEAD = 1) the VCA assigns the 24 MSBs of the Virtual Channel Frame Counter to the Secondary Header Data field.

MSB	32-bit Virtual Channel Frame Counter			LSB
0		23	24	31

MSB	Secondary Header Data	LSB	MSB	VC Frame Count	LSB
0		23	0		7

3.7 First Header Pointer

The First Header Pointer is required for the Telemetry Packet chaining process during Telemetry Packet de-multiplexing on the ground. The VCA generates partial Transfer Frames in one of two possible states; **active** or **idle**, as defined in RD1. The data contained in an **active** Transfer Frame can be either Telemetry Packets (SYNCF = 0) or non-packet data delimited into data blocks (SYNCF = 1). Telemetry Packets are referred to as **synchronous** data in RD1 whereas non-packet data are referred to as **asynchronous** data.

In the **active** state, Telemetry Packets may be of varying lengths. It is unlikely that an integer number of Telemetry Packets will be exactly contained within a Transfer Frame, so some Telemetry Packets will be split between two Transfer Frames. The VCA calculates the position of the first octet of the first Telemetry Packet to be placed in each Transfer Frame, in accordance with RD1, then inserts this value into the header of the PVCF.

For the VCA, the above also applies to non-packet data, allowing data blocks to be identified in the data stream. This is an extension to RD1, permitting the First Header Pointer also to be set for non-packet data in the same way as it is set for Telemetry Packets. This feature is activated by using the VPD* signal for the parallel input interface (SVALID signal for the serial interface) to delimit data blocks, in the same way as for delimiting Telemetry Packets. For serial input mode SVALID has the same functions as VPD* in parallel input mode.

The First Header Pointer is initiated to "all ones" at reset, allowing the VCA to operate in full compliance with RD1 for non-packet data by permanently connecting VPD* to logic 0 (SVALID to logic 1 when SMODE = 1). This means that when using Telemetry Packets (or when using the First Header Pointer for non-packet data), the VPD* input should be held at logic 1 (SVALID at logic 0 when SMODE = 1) until six CLK cycles after RESET* has been de-asserted, to be de-asserted before writing the first Telemetry Packet or data block. Otherwise the First Header Pointer for the first transmitted non-Idle Transfer Frame after reset would have the First Header Pointer set to "all ones" instead of "all zeroes".

If VPD* (SVALID when SMODE = 1) was not de-asserted while all the data filling up a Transfer Frame was input, e.g. if a Telemetry Packet or data block is longer than the data field of the Transfer Frame, the First Header Pointer is set to "all ones"; First Header Pointer = 11111111111.

In the **idle** state the VCA sends a partial Idle Transfer Frame and the First Header Pointer is set to the predefined Idle First Header Pointer code. This code is the same both for Telemetry Packets and non-packet data; First Header Pointer = 11111111110.

The VCA fully supports the First Header Pointer and has therefore no requirements on aligning the data with the Transfer Frame boundary, contrary to other implementations.

3.8 VCA/VCM interface

The VCA/VCM interface, shown in figure 5, is for the serial transfer of partial Transfer Frames to the VCM. The VCA relates its operations to the rising CLK edge (rising BITCLK edge, when CLKMODE = 1), whereas the VCM relates its operations to the falling BITCLK edge, to minimize potential skew problems. The VCA has a Clear To Send (CTS) and a device POLLed (POLL) input, and a Ready To Send (RTS) and a Partial Virtual Channel Frame data (PVCF) output.

The VCA/VCM interface can operate relative to the BITCLK signal for bit rates up to 3 MBit/s or relative to the CLK signal for bit rates up to 12.5 MBit/s. When CLKMODE = 0 the VCA/VCM interface uses the CLK signal; when CLKMODE = 1 the interface uses the asynchronous BITCLK signal. BITCLK is then sampled internally by the VCA generating an internal enable signal when the rising BITCLK edge is detected. This signal enables the interface signals (RTS, POLL, CTS, PVCF) to be sampled/driven during the next CLK cycle.

Using the BITCLK signal enables the VCA to operate at a higher clock frequency than the VCM, allowing a bit rate independent input data rate. In addition, the RAM power dissipation might decrease due to the chip select being asserted for a shorter time, depending on the RAM device used.

The VCA asserts the output signal RTS when it has stored a complete PVCF in RAM. RTS will remain asserted as long as there is one or more complete PVCFs in RAM, excluding a PVCF currently being output. When the VCM is ready to receive data from the VCA, it asserts the CTS signal. Three CLK (or BITCLK) cycles, after the VCA has detected the asserted CTS input it will start to output PVCF data. The PVCF data are output at the rate of one bit per CLK (or BITCLK) cycle without interrupt until the complete PVCF has been output. The CTS input shall be asserted for a minimum of 16 CLK cycles, and it shall be de-asserted before the end of the PVCF.

If the VCM asserts the CTS signal when the VCA has not asserted RTS, the VCA outputs an Idle PVCF. Refer to section 2.2 for the PVCF format. The POLL input is described in section 3.10.

3.9 Idle Transfer Frames

An Idle PVCF, which will be finalized into an Idle Transfer Frame by the VCM, will be produced when the VCA has not stored a complete PVCF in RAM, when CTS is asserted. Idle PVCFs are not stored in RAM but generated while being output. The timing and the length of an Idle PVCF is identical to a normal PVCF. Idle Transfer Frames should not be confused with Idle Telemetry Packets.

The Idle PVCF Data Field contains no useful data; it will be filled with data from the Idle Fill data input (IFILL). One bit per CLK cycle (BITCLK cycle, when CLKMODE = 1) is sampled and used for Idle PVCF data.

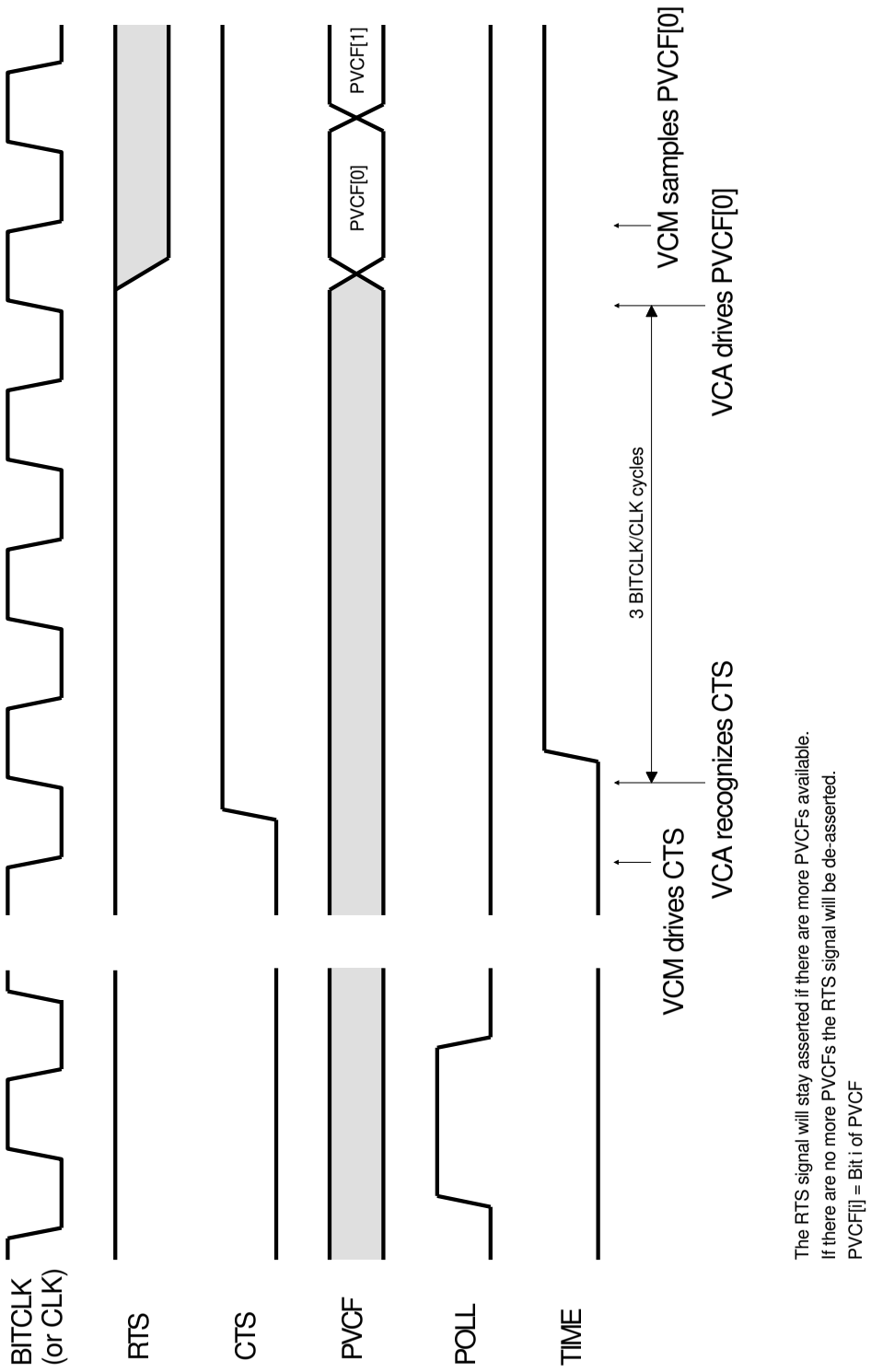

Figure 5: Timing of VCA/VCM interface

3.10 Idle Telemetry Packet insertion

The VCA can optionally generate and insert Idle Telemetry Packets, to fill up an incomplete Transfer Frame. This ensures that Telemetry Packets do not remain inaccessible due to an incomplete Transfer Frame being resident in the RAM. This feature is only available when the VCA is operating with Telemetry Packets, referred to as **synchronous** data in RD1. Idle Telemetry Packets should not be confused with Idle Transfer Frames.

The Idle Telemetry Packet insertion process starts when all of the following conditions are met:

- The VCA operates with Telemetry Packets (SYNCF = 0).
- The source is not sending a Telemetry Packet (VPD* = 1 or SVALID = 0, respectively).
- The VCA is not Ready To Send data (RTS = 0).
- An incomplete PVCF (containing non-Idle Telemetry Packets or part of a non-Idle Telemetry Packet) is resident in the external RAM.
- The value of the Poll Program inputs, PPROG0 - PPROG2, is not equal to 111.
- The appropriate number of device polls have been counted by the Poll Counter, as described in 3.10.1.

When the Idle Telemetry Packet insertion process has filled the PVCF, the VCA asserts the RTS output. The Idle Telemetry Packet insertion process stops after the last Idle Telemetry Packet has been stored in the RAM. In the case that the last Idle Telemetry Packet spilled over, it will be written to the next PVCF. The time required for the VCA to complete a PVCF with Idle Telemetry Packets depends on how much space there is left to be filled. The worst case is when the longest possible data field in a Transfer Frame of 1115 octets contains only one octet of Telemetry Packet data, which will take less than 12 000 CLK cycles to complete the PVCF data field.

Should VPD* (SVALID when SMODE = 1) be asserted after the Idle Telemetry Packet insertion process has started, the current Idle Telemetry Packet is completed in parallel with the storing of Telemetry Packet data and then the Idle Telemetry Packet insertion process is suspended. As soon as VPD* (SVALID) is de-asserted, indicating the end of the normal Telemetry Packet, the Idle Telemetry Packet insertion process resumes and continues until the PVCF has been completed (it will not stop due to a new Telemetry Packet being received) unless the PVCF was already completely filled with normal Telemetry Packets.

The VCA is able to receive Telemetry Packets and send PVCFs simultaneously with the insertion of an Idle Telemetry Packet.

When a Transfer Frame contains no Telemetry Packets or when it contains only part of an Idle Telemetry Packet, the Idle Telemetry Packet insertion process will not start. The situation where a PVCF contains only part of an Idle Telemetry Packet occurs when an Idle Packet spilled over from the previous Transfer Frame and it is the only data in the Transfer Frame.

3.10.1 Poll Counter

In the previous section six conditions were listed for the Idle Telemetry Packet insertion process to commence. When the VCA detects that the first five conditions are met it enables the Poll Counter. The Poll Counter is reset and disabled when either of the following conditions is met:

- The source asserts VPD* or SVALID in preparation for sending Telemetry Packets, OR
- The Idle Telemetry Packet insertion process is active.

When the Poll Counter is enabled it increments by one at every rising CLK edge (rising BITCLK edge, when CLKMODE = 1) when the POLL input is asserted. The VCM asserts POLL every time it checks the RTS signal of the VCA, while selecting which VCA to output the next PVCF. The Poll Counter increments until it reaches the number of programmed polls, ranging from 1 to 1024, as indicated by the value of PPROG0 - PPROG2 and then it enables the Idle Telemetry Packet insertion process. Section 4.6.9 defines the interpretation of the PPROG inputs.

The Poll Counter is enabled when:
(SYNCF = 0) AND
(VPD* = 1 or SVALID = 0, respectively) AND
(RTS = 0) AND
(000 < PPROG[0..2] < 111) AND
(the incomplete PVCF contains non-Idle Telemetry Packet data) AND
(the Idle Telemetry Packet insertion process is not active)
otherwise the Poll Counter is reset and disabled

The Poll Counter is incremented by one at every rising CLK edge (rising BITCLK edge, when CLKMODE = 1) when:
(Poll Counter enabled) AND (POLL = 1)

The Idle Telemetry Packet insertion process starts when:
((Poll Counter enabled) AND
(Poll Counter = Threshold value as defined in 4.6.9)) OR
((PPROG[0..2] = 000) AND
(SYNCF = 0) AND
(VPD* = 1) AND
(RTS = 0) AND
(the incomplete PVCF contains non-Idle Telemetry Packet data))

The Idle Telemetry Packet insertion process stops when:
The PVCF is complete and the remainder of the last Idle Telemetry Packet has been stored in the next PVCF, if the Idle Telemetry Packet spills over from the last PVCF.

The relation between the signals POLL and VPD* or SVALID has to allow for internal synchronization of the signals in the VCA.

3.10.2 Idle Telemetry Packet

The VCA generates the Idle Telemetry Packet Header and inserts the pre-defined values, as described in section 2.3, into the appropriate fields.

The data field of an Idle Telemetry Packet is filled with data from the Idle Fill data input (IFILL). One bit per CLK cycle is sampled and used for Idle Telemetry Packet data.

3.11 Pseudo-random Idle Fill data

The Pseudo-random Idle Fill data are generated to provide fill data for the data fields of Idle Telemetry Packets and Idle PVCFs. The pseudo-random data generator generates the RANDOM output signal, which can be connected to the Idle Fill data input pin (IFILL). The data output rate is one bit per CLK cycle. The pseudo-random data generator is free-running, and will not be initialized by any event except reset (RESET* = 0). The pseudo-random data generator polynomial is $x^9 + x^5 + 1$

The design of the generator ensures that a Single Event Upset (SEU) or any other spurious event will not cause the generator to jump to an invalid state and produce a continuous output of ones or zeros.

3.12 Time sampling strobe

The VCA provides the active high TIME strobe for sampling the on-board time according to section 7.4 of RD1. TIME is asserted one CLK cycle (two CLK cycles after the rising BITCLK edge, when CLKMODE = 1) after CTS has been asserted, when the eight LSBs of the Virtual Channel Frame Counter for the partial Transfer Frame to be sent out contain the value(s) selected by the four TMODE pins as defined in section 4.6.10. This allows all intervals defined in RD1 to be selected. TIME will remain asserted for 128 CLK cycles, regardless of the CLKMODE value.

This means that the TIME strobe will be asserted 51 CLK cycles (51 BITCLK plus two CLK cycles after the rising BITCLK edge, when CLKMODE = 1) after the leading edge of the Synchronisation Marker has been output from the VCM. This can be regarded as compliant with the requirements of RD1 since the delay relative to the rising edge of the first bit of the Synchronisation Marker is fixed and known.

If it nevertheless is required to sample the on-board time exactly at the rising edge of the Synchronisation Marker, the time can be sampled at this edge for every Transfer Frame generated but only read out when the TIME strobe is asserted.

The TIME strobe from the VCA associated with Virtual Channel 0 should be used for sampling the on-board spacecraft time.

3.13 Test

The VCA features Built-In Self Test (BIST) with a fault coverage of 89.5 %. The BIST runs for 4996 CLK cycles after RESET* has been released. The BIST result does not depend on the state of any of the inputs. The BIST can be disabled by connecting the TEST0 input to logic 1; after releasing RESET* the VCA will be reset but no BIST will be performed.

If an error is detected by the BIST, the ERR* output remains asserted (ERR* = 0), until the next reset occurs. The VCA will try to continue to operate in normal mode. If no internal error was detected the ERR* output is de-asserted, and the VCA starts working in normal mode.

When RESET* is asserted and during BIST, the RCS*, OE* and R/W* outputs are driven to logic 1 and all other outputs except RANDOM are driven to logic 0 so as not to trigger connected devices. The RD data bus is driven to 0 to ensure that it is not left floating. Due to design reasons, the RANDOM pin outputs pseudo-random data also during BIST.

The active high input External Ram Test (ERT) can be used to tristate all outputs from the VCA to the external RAM, to allow for RAM test. When ERT is asserted the outputs ERR*, VCAR and RTS are held at logic 0 since the VCA no longer can control the RAM. When ERT is de-asserted control of the RAM interface, VCAR, RTS and ERR* is returned to the VCA. ERT is asynchronous and only disables the outputs, without any other impact on the VCA.

The production test for the VCA has a fault coverage higher than 96 %, and is performed at a CLK frequency of 10 MHz. The TEST1 input is used for the production test and shall be tied to logic 0 during normal operation.

The fault coverage figures are based on stuck-at-0/1 faults at the gate level, faulting all nets (gate outputs).

3.14 State after reset

After reset, or after reset and completion of BIST, the VCA is initialized as follows:

- The Virtual Channel Frame Counter has the value 0.
- The First Header Pointer is initialized in accordance with section 3.7.
- The Poll Counter has the value 0.

Since the VCA BIST takes fewer CLK cycles than the VCM BIST, the VCA will always be ready when the VCM requires the first Transfer Frame (except for the unrealistic case when the VCA performs BIST and the VCM does not).

4 INTERFACE AND SIGNAL DESCRIPTION

The VCA has 41 input signals, 24 output signals and 8 bidirectional signals. Together with 10 power supply pins and one NC pin, this gives a total pin count of 84. The character * is used to indicate an active low signal.

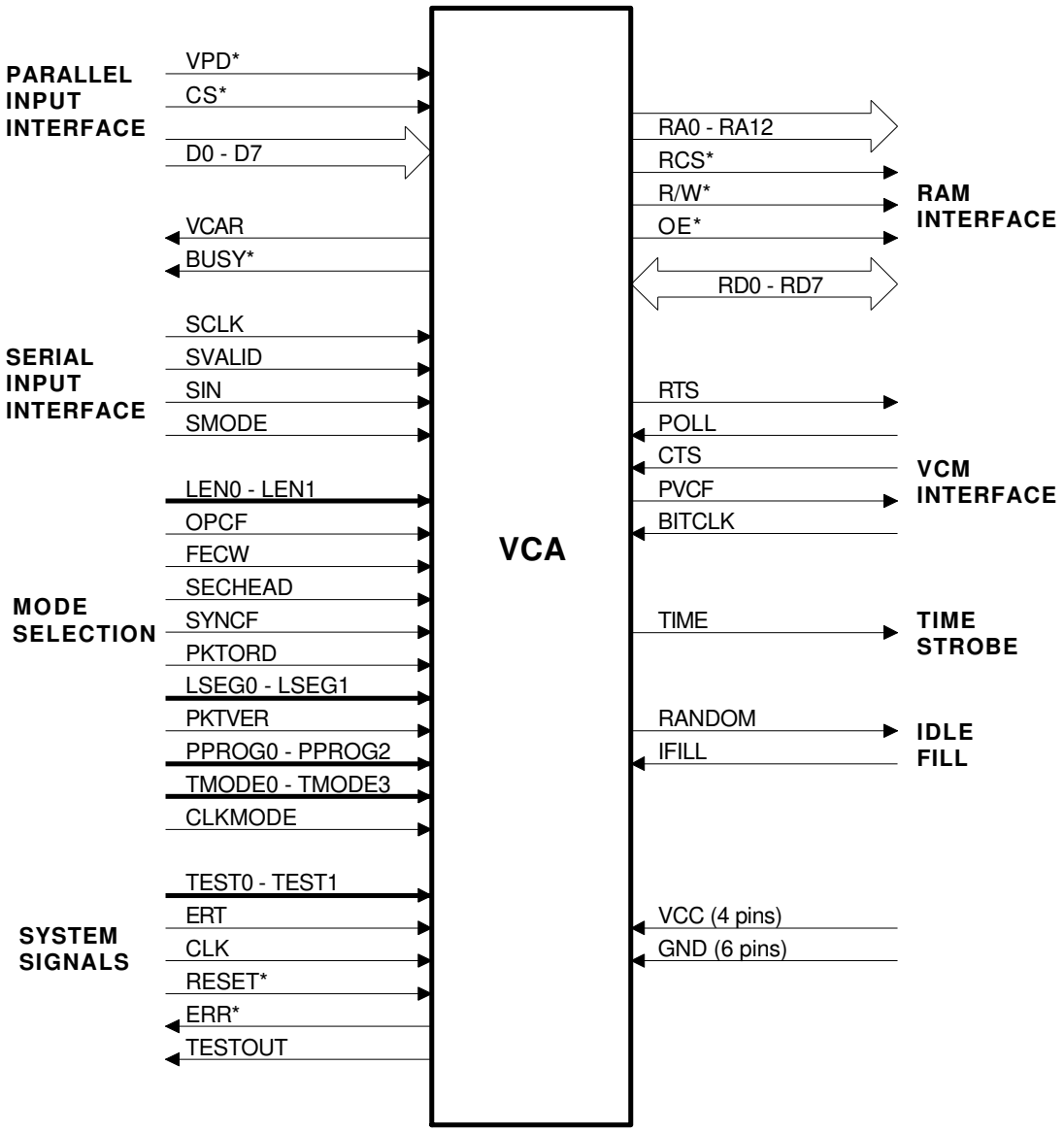

Figure 6: Signal overview

4.1 Parallel input interface, 12 pins

4.1.1 VPD*: Valid Packet Data for parallel interface (I)

This asynchronous TTL input informs the VCA when a Telemetry Packet (data block in **asynchronous** mode) begins/ends. VPD* shall be asserted (= 0) while the source is transferring data and shall not change state while CS* is asserted.

4.1.2 CS*: Parallel interface Chip Select (I)

This asynchronous TTL input is used to latch data into the VCA. Data are latched on the rising CS* edge. The maximum input data rate is one octet per four CLK cycles.

4.1.3 D0 - D7: Parallel Data input (I)

These TTL inputs contain data from the source. The VCA latches data from these signals on the rising CS* edge, when VPD* is asserted. Note: D0 is the MSB.

4.1.4 VCAR: VCA Ready (O)

This output is asserted (= 1) when the VCA has place to store data in the external RAM, as defined below. VCAR changes state on the falling CLK edge. VCAR is also de-asserted when ERT is asserted (= 1) since the RAM is then not accessible. The values correspond to one maximum length packet or data field, respectively.

SYNCF	LSEG0	LSEG1	VCAR Threshold
0	0	0	≥ 262 (256 + 6)
0	0	1	≥ 518 (512 + 6)
0	1	0	≥ 1030 (1024 + 6)
0	1	1	≥ Length of Transfer Frame Data Field
1	-	-	≥ Length of Transfer Frame Data Field

4.1.5 BUSY*: VCA Busy (O)

This output is asserted immediately after an octet has been input to the VCA, and is asserted until the octet has been stored in the external RAM. BUSY* is asserted on the rising CS* edge and is de-asserted on the falling CLK edge.

4.2 Serial input interface, 4 pins

The VCAR and BUSY* outputs have the same functions as described in section 4.1.4 and section 4.1.5, respectively.

4.2.1 SCLK: Serial interface clock (I)

This asynchronous CMOS input is used to clock serial data into the VCA. The maximum input data rate is one octet per four CLK cycles.

4.2.2 SVALID: Serial interface data Valid (I)

This asynchronous CMOS input informs the VCA when a Telemetry Packet (data block in **asynchronous** mode) begins/ends and defines the octet boundaries in the data stream, the first octet explicitly and the following octets each subsequent eight SCLK cycles. SVALID shall be asserted while data are input.

4.2.3 SIN: Serial interface data input (I)

This CMOS input contains data from the source. The VCA samples SIN on the rising SCLK edge, when SVALID is asserted.

4.2.4 SMODE: Serial Mode (I)

This static CMOS input selects the serial or parallel input interface, the serial interface is selected when SMODE = 1.

4.3 RAM interface, 24 pins

4.3.1 RA0 - RA12: RAM Address (O)

These outputs are the addresses generated by the VCA for reading and writing to the external RAM. RA0 - RA12 change state on the rising CLK edge and are tristated when ERT is asserted.

4.3.2 RCS*: RAM Chip Select (O)

This active low output is the Chip Select for the external RAM. RCS* changes state on the falling CLK edge and is tristated when ERT is asserted.

4.3.3 R/W*: RAM Read/Write Control (O)

This output is the Read/Write control for the external RAM. R/W* changes state on the falling CLK edge and is tristated when ERT is asserted.

4.3.4 OE*: RAM Output Enable Control (O)

This active low output is the Output Enable control for the external RAM. OE* changes state on the falling CLK edge and is tristated when ERT is asserted.

4.3.5 RD0 - RD7: RAM Data (I/O)

These TTL level signals are used to read and write data to the external RAM. RD0 - RD7 are driven by the VCA on the falling CLK edge and are tristated on the rising CLK edge. These signals are also tristated when ERT is asserted.

4.4 VCM interface, 5 pins

4.4.1 RTS: Ready To Send (O)

This output is asserted when at least one complete PVCF is available to be output. RTS changes state on the rising CLK edge when CLKMODE = 0 and on the rising BITCLK edge when CLKMODE = 1. RTS is also de-asserted when ERT is asserted (= 1), since the RAM is then not accessible and no PVCF can be output.

4.4.2 POLL: Device Poll (I)

This CMOS level input is asserted by the VCM every time it senses the RTS signal of the VCA. POLL shall be valid at the rising CLK edge when CLKMODE = 0 and at the rising BITCLK edge when CLKMODE = 1.

4.4.3 CTS: Clear To Send (I)

This CMOS level input is used by the VCM to request a PVCF to be output from the VCA. CTS shall be valid at the rising CLK edge when CLKMODE = 0 and at the rising BITCLK edge when CLKMODE = 1.

4.4.4 PVCF: Partial Virtual Channel Frame data (O)

This output is the PVCF output data. PVCF changes state on the rising CLK edge when CLKMODE = 0 and on the rising BITCLK edge when CLKMODE = 1.

4.4.5 BITCLK: Bit clock (I)

This asynchronous CMOS input is used to define the bit clock for the VCA/VCM interface when CLKMODE = 1, otherwise it shall be connected to a defined logic level. The maximum frequency is the CLK frequency divided by four.

4.5 Time sampling strobe, 1 pin

4.5.1 TIME: Time sampling strobe (O)

This output is asserted to indicate that the on-board time should be sampled and sent to the ground in a Telemetry Packet. TIME changes state on the rising CLK edge when CLKMODE = 0 and on the rising CLK edge two CLK cycles after a rising BITCLK edge is detected when CLKMODE = 1.

4.6 Operational mode selection, 18 pins

4.6.1 LEN0, LEN1: Transfer Frame Length (I)

These static CMOS inputs define the length of the Transfer Frame and the length of the space for the Reed-Solomon check codes:

LEN0	LEN1	Transfer Frame length	Length of space for check codes
0	0	223 octets	32 octets
0	1	446 octets	64 octets
1	0	892 octets	128 octets
1	1	1115 octets	160 octets

4.6.2 OPCF: Operational Control Field (I)

This static CMOS input specifies whether an Operational Control Field is present in the Transfer Frame Trailer (OPCF = 1). The VCA does not generate the Transfer Frame Trailer, but adjusts the PVCF length.

4.6.3 FECW: Frame Error Control Word (I)

This static CMOS input specifies whether a Frame Error Control Word is present in the Transfer Frame Trailer (FECW = 1). The VCA does not generate the Transfer Frame Trailer, but adjusts the PVCF length.

4.6.4 SECHEAD: Secondary Header Flag (I)

This static CMOS input specifies whether a Secondary Header should be generated (SECHEAD = 1) and inserted into the PVCF.

4.6.5 SYNCF: Synchronisation Flag (I)

This static CMOS input specifies whether input data are standard Telemetry Packets (referred to as **synchronous** mode in RD1, SYNCF = 0) or non-packet data (referred to as **asynchronous** mode in RD1, SYNCF = 1).

4.6.6 PKTORD: Packet Order Flag (I)

This static CMOS input specifies the value of the Packet Order Flag in the PVCF Header. Packet sequence count/segmentation order is **forward** when PKTORD = 0 and **reverse** when PKTORD = 1. Except for the value of this field, PKTORD has no impact on the VCA operation.

4.6.7 LSEG0, LSEG1: Segmentation Length Identifiers (I)

These static CMOS inputs specify the maximum segment length of Telemetry Packets. Note that the VCA does not perform segmentation, it should be performed by the source.

LSEG0	LSEG1:	Maximum Data Field length of Telemetry Packets
0	0	256 octets
0	1	512 octets
1	0	1024 octets
1	1	65536 octets (no segmentation)

4.6.8 PKTVER: Packet version for Idle Telemetry Packets (I)

This static CMOS input specifies the version of the Idle Telemetry Packet. PKTVER = 0 results in version 1 packets (Version field = 000), PKTVER = 1 results in version 2 packets (Version field = 100) which is compliant with RD1.

4.6.9 PPROG0 - PPROG2: Poll Program (I)

These CMOS inputs define the number of POLL assertions to be counted before the Idle Telemetry Packet insertion process starts. For direct control of when Idle Telemetry Packets shall be inserted independent of the POLL input, all PPROG signals can be tied together and when set to logic 0 for more than two CLK cycles the Idle Telemetry Packet insertion process starts, provided that the conditions described in section 3.10.1 are fulfilled.

These inputs should be static except when used to enable immediate Idle Telemetry Packet generation.

PPROG2	PPROG1	PPROG0	Poll Counter Threshold
0	0	0	Immediate Idle Telemetry Packet insertion [1]
0	0	1	1 device poll
0	1	0	4 device polls
0	1	1	16 device polls
1	0	0	64 device polls
1	0	1	256 device polls
1	1	0	1024 device polls
1	1	1	Idle Telemetry Packet insertion process will not be started

1) Idle Telemetry Packet insertion process starts when the conditions in section 3.10.1 are met.

4.6.10 TMODE0 - TMODE3: Timing strobe Mode (I)

These static CMOS inputs are used to set the interval for asserting the TIME strobe, in accordance with section 7.4 of RD1. The sampling interval of 256 frames corresponds to the assertion of TIME for each partial Transfer Frame with the Virtual Channel Count LSB value of 0. Similarly, the sampling interval of 1 frame corresponds to the Virtual Channel Count LSB values of 0, 1, 2, 3, 4 ... 253, 254 and 255.

TMODE0	TMODE1	TMODE2	TMODE3	Virtual Channel Count LSB value(s)
0	0	0	0	0, 1, 2, 3, 4 ... 253, 254, 255
0	0	0	1	0, 2, 4, 6, 8 ... 250, 252, 254
0	0	1	0	0, 4, 8, 12, 16 ... 244, 248, 252
0	0	1	1	0, 8, 16, 24, 32 ... 232, 240, 248
0	1	0	0	0, 16, 32, 48, 64 ... 208, 224, 240
0	1	0	1	0, 32, 64, 96, 128, 160, 192, 224
0	1	1	0	0, 64, 128, 192
0	1	1	1	0, 128
1	0	0	0	0

4.6.11 CLKMODE: Clock Mode (I)

This static CMOS input selects whether the VCA/VCM interface uses the CLK signal (CLKMODE = 0) or the BITCLK signal.

4.7 Miscellaneous, 20 pins

4.7.1 TEST0, TEST1: Test mode (I)

These static CMOS inputs are used to set the VCA in test modes. TEST0 is used for controlling the internal BIST, which will be performed after reset when TEST0 = 0. TEST1 is used for production test and should always be tied to logic 0.

4.7.2 ERT: External RAM Test (I)

This asynchronous CMOS input is used to tristate all the signals from the VCA to the external RAM, to allow for board testing. For normal operation ERT is de-asserted (ERT = 0) and the VCA controls the RAM interface signals. When ERT = 1, the VCA tristates all signals to the RAM.

4.7.3 CLK: Clock (I)

This CMOS input is the clock signal for the VCA.

4.7.4 RESET*: Master Reset (I)

This asynchronous Schmitt trigger input resets the VCA. The BIST is activated after the rising RESET* edge if the input TEST0 = 0. After the BIST is completed all registers are reset and the VCA starts with normal operation.

4.7.5 ERR*: Internal Error (O)

This output indicates that an internal error has been detected. During reset and BIST ERR* is asserted (= 0). If no error was detected during the self-test ERR* is de-asserted. ERR* changes state on the falling CLK edge. In addition, ERR* is asserted asynchronously when ERT is asserted, since the RAM is not accessible.

4.7.6 TESTOUT: Production Test Output (O)

This output is used for production test purposes only and should not be connected.

4.7.7 RANDOM: Pseudo-random Data (O)

This output is used to output pseudo-random data. RANDOM changes state on the rising CLK edge and is intended to be connected to the IFILL input pin.

4.7.8 IFILL: Idle Fill Data (I)

The data applied to this CMOS input is inserted into the data field of an Idle Transfer Frame or an Idle Telemetry Packet. IFILL shall be valid at the falling CLK edge.

4.7.9 VCC and GND: Power supply

Four pins for VCC and six pins for GND.

4.7.10 NC: Not Connected

This pin is not bonded. It could e.g. be connected to GND or left unconnected.

5 ELECTRICAL AND MECHANICAL DATA

The VCA has been designed for the full military temperature range in the ABB Hafo SOS4 2 µ CMOS/SOS process. The die has an area of 91 mm^2 and contains 33k transistors. The VCA is a fully static design.

Note: the parameters in this section are preliminary and are subject to change.

5.1 Absolute maximum ratings

Storage temperature	-65 °C to +150 °C
Operating ambient temperature	-55 °C to +125 °C
Supply voltage, V_{CC}	-0.5 V to +7.0 V
Input voltage	-0.5 V to V_{CC} + 0.5 V
DC input current (any pin)	±20 mA
Power dissipation	200 mWdc
Output dissipation	50 mWdc/output
ESD minimum critical path failure voltage	1500 V [1]
Total dose tolerance	> 100 kRad (Si)
Latch-up	Immune

1) Categorized as Class 2.

5.2 DC specifications

Valid over the full functional operating range; V_{CC} = 5 V ± 10%, T_{CASE} = -55 °C to +125 °C, after 100 kRad irradiation.

Parameter	Min	Max	Condition
CMOS inputs:			
Input low voltage	0.0 V	1.3 V	
Input high voltage	3.9 V	V_{CC}	
Input leakage current		±10 µA	CLK input, $0 \le V_{IN} \le V_{CC}$
Input leakage current		±1 µA	Other inputs, $0 \le V_{IN} \le V_{CC}$
Capacitance [1]		15 pF	CLK input
Capacitance [1]		5 pF	Other inputs
TTL inputs:			
Input low voltage	0.0 V	0.8 V	
Input high voltage	2.0 V	V_{CC}	
Input leakage current		±1 µA	$0 \le V_{IN} \le V_{CC}$
Capacitance [1]		5 pF	

Parameter	Min	Max	Condition
Schmitt trigger inputs:			
Input low trigger voltage		1.0 V	
Input high trigger voltage	V_{CC}-1.2 V		
Schmitt trigger hysteresis	0.5 V		
Input leakage current		±1 µA	$0 \le V_{IN} \le V_{CC}$
Capacitance [1]		5 pF	
Outputs: [2]			
Output low voltage		0.40 V	I = 4 mA
Output high voltage	V_{CC}-0.6 V		I = 4 mA
Output leakage current		20 µA	Tristate, $0 \le V_{OUT} \le V_{CC}$
Capacitance [1]		10 pF	
TTL Bidirectional signals:			
Input low voltage	0.0 V	0.8 V	
Input high voltage	2.0 V	V_{CC}	
Output low voltage		0.40 V	I = 4 mA
Output high voltage	V_{CC}-0.6 V		I = 4 mA
Output leakage current		20 µA	Tristate, $0 \le V_{OUT} \le V_{CC}$
Capacitance [1]		10 pF	
Power dissipation: [3]			
Static dissipation [4]		25 mW	
Dynamic dissipation		10 mW/MHz	Normal operation
Dynamic dissipation		35 mW/MHz	During BIST
TTL input [5]		0.05 mW/input	V_{IN} = 0.8 V
TTL input [5]		3.5 mW/input	V_{IN} = 2.4 V

1) Capacitance values include the pad and the pin.

2) The outputs are compatible with both CMOS and TTL level inputs.

3) With 25 pF load on all outputs. The total power dissipation is the sum of the static dissipation, the dynamic dissipation at the operational frequency and the TTL input dissipation.

4) The high value for the static dissipation is due to the leakage current at high temperatures.

5) The TTL dissipation depends on the input voltage and is close to zero when the input is held at 0 V or V_{CC}. TTL level inputs should therefore be driven as close as possible to the end voltages.

5.3 AC specifications

All timing values are valid for the full operational temperature range, radiation range and power supply range, with 25 pF output load (add 8 ns to the output delays for 50 pF load).

No.	Description	Min	Max
T_{RES}	RESET* asserted	4 T_{CLK}	
f_{CLK}	CLK frequency	0 Hz	12.5 MHz
T_{CLK}	CLK period	80 ns	
T_{CLO}	CLK low	40 ns	
T_{CHI}	CLK high	40 ns	
f_{BCK}	BITCLK frequency	0 Hz	f_{CLK} / 4
T_{BCK}	BITCLK period	4 • T_{CLK}	
T_{BLO}	BITCLK low	4 • T_{CLO}	
T_{BHI}	BITCLK high	4 • T_{CHI}	
f_{SCK}	SCLK frequency [1]	0 Hz	f_{CLK} • 2
T_{SCK}	SCLK period	T_{CLK} / 2	
T_{SLO}	SCLK low	20 ns	
T_{SHI}	SCLK high	20 ns	
T_1	CS* cycle time	4 T_{CLK}	
T_2	VPD* asserted to CS* asserted	5 ns	
T_3	CS* width asserted	30 ns	
T_4	CS* width de-asserted	30 ns	
T_5	CS* de-asserted to VPD* de-asserted	0 ns	
T_6	VPD* width de-asserted	2 T_{CLK}	
T_7	D setup time	8 ns	
T_8	D hold time	15 ns	
T_9	CS* de-asserted to BUSY* asserted		35 ns
T_{10}	BUSY* width asserted	3 T_{CLK}	4 T_{CLK}
T_{11}	CS* de-asserted to VCAR de-asserted	2.5 T_{CLK}	3.5 T_{CLK}
T_{12}	CLK low to VCAR valid [2]		30 ns
T_{13}	ERT high to VCAR low		20 ns
T_{14}	ERT low to VCAR valid		30 ns
T_{15}	SVALID high to SCLK high	50 ns	
T_{16}	SCLK high to SVALID low	50 ns	
T_{17}	SVALID width de-asserted	2 T_{CLK}	
T_{18}	SIN setup time	5 ns	
T_{19}	SIN hold time	15 ns	

No.	Description	Min	Max
T_{20}	CLK high to RA valid		30 ns
T_{21}	CLK low to RCS* valid		30 ns
T_{22}	CLK low to R/W* low		30 ns
T_{23}	CLK low to R/W* high		30 ns
T_{24}	CLK low to OE* low		30 ns
T_{25}	CLK low to OE* high		30 ns
T_{26}	CLK low to RD write data valid		40 ns
T_{27}	CLK high to RD tristate		40 ns
T_{28}	Read data setup time	18 ns	
T_{29}	OE*/RCS* high to RD invalid	0 ns	
T_{30}	ERT high to RA, RCS*, R/W*, OE*, RD tristate		25 ns
T_{31}	ERT low to RA, RCS*, R/W*, OE*, RD valid		30 ns
T_{32}	CLK low to ERR* valid		30 ns
T_{33}	ERT high to ERR* low		20 ns
T_{34}	ERT low to ERR* valid		30 ns
T_{35}	ERT high to RTS low		20 ns
T_{36}	ERT low to RTS valid		30 ns
T_{37}	CLK high to RTS stable [3]		31 ns
T_{38}	CTS setup time [4]	6 ns	
T_{39}	CLK high to PVCF stable [3]		30 ns
T_{40}	POLL setup time [4]	5 ns	
T_{41}	POLL hold time [4]	10 ns	
T_{42}	CLK high to TIME asserted [5]		30 ns
T_{43}	CLK high to RANDOM valid		30 ns
T_{44}	IFILL setup time	10 ns	
T_{45}	IFILL hold time	5 ns	

1) Only tested to 20 MHz.

2) T_{12} is not shown in the timing waveforms.

3) When CLKMODE = 1, this occurs after the rising BITCLK edge.

4) When CLKMODE = 0, CLK is used. When CLKMODE = 1, BITCLK is used and it may be asynchronous, being internally synchronized.

5) When CLKMODE = 1, TIME is asserted on the rising CLK edge two CLK cycles after the rising BITCLK edge.

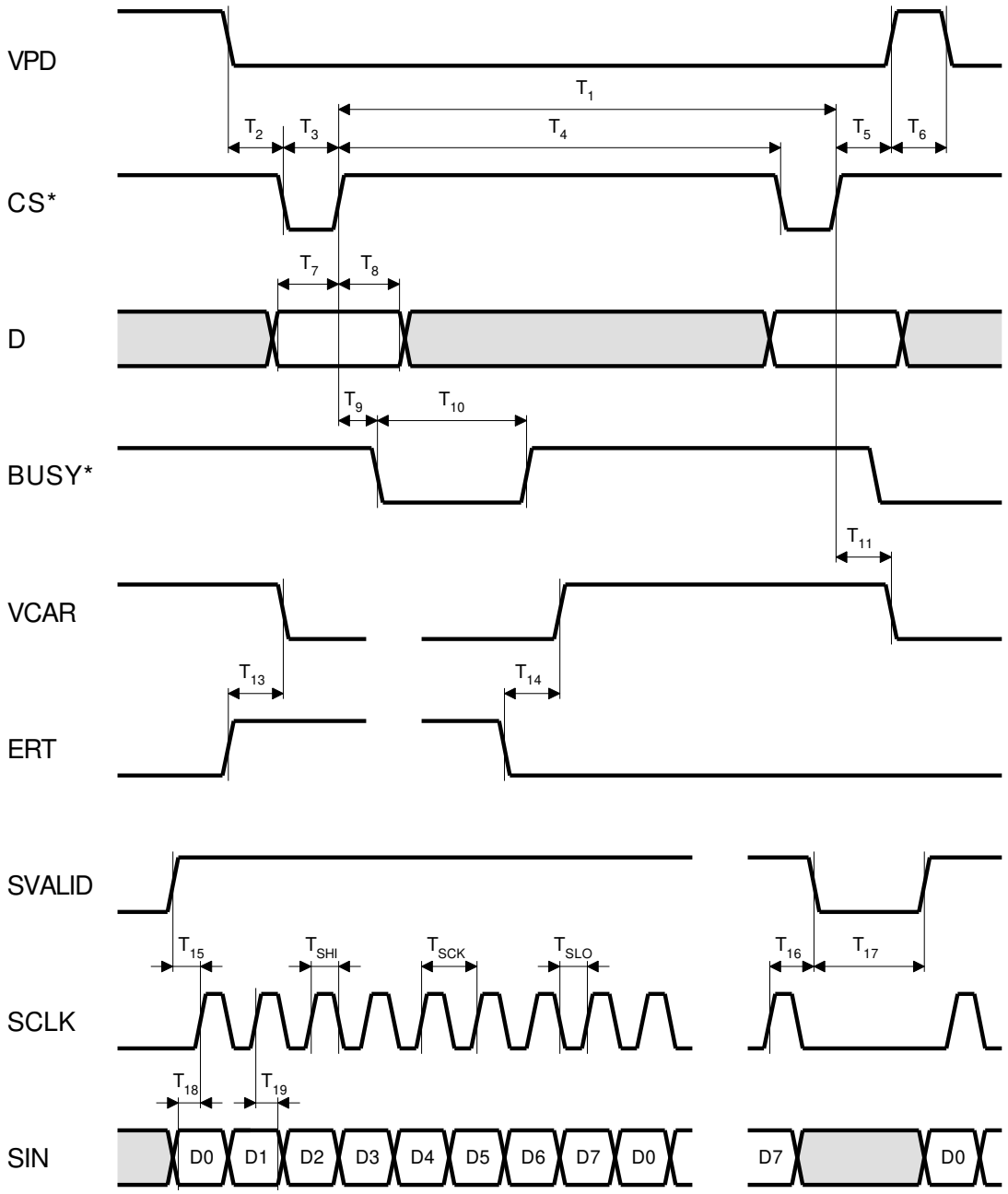

Figure 7: Timing of various signals

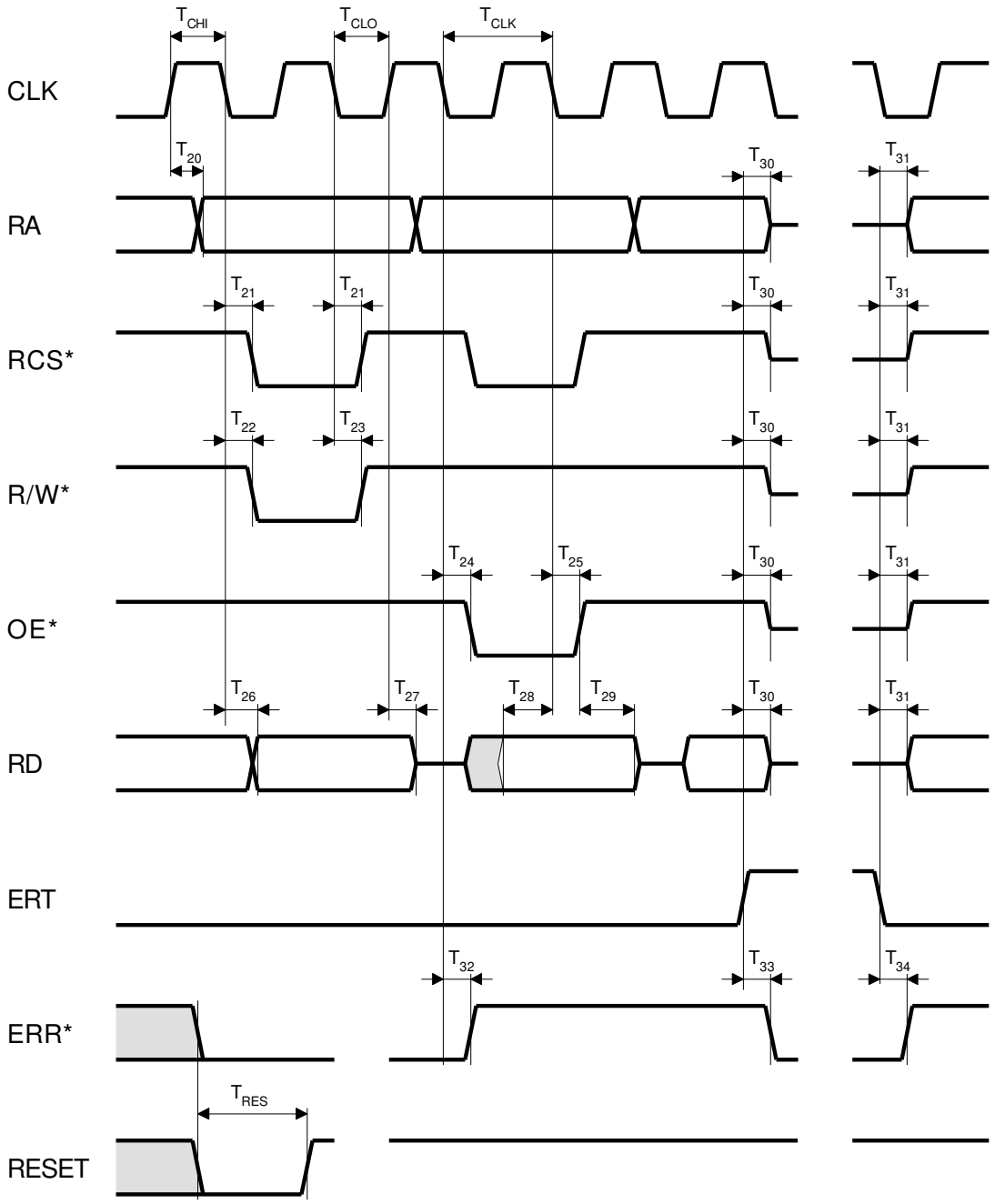

Figure 8: Timing of various signals (continued)

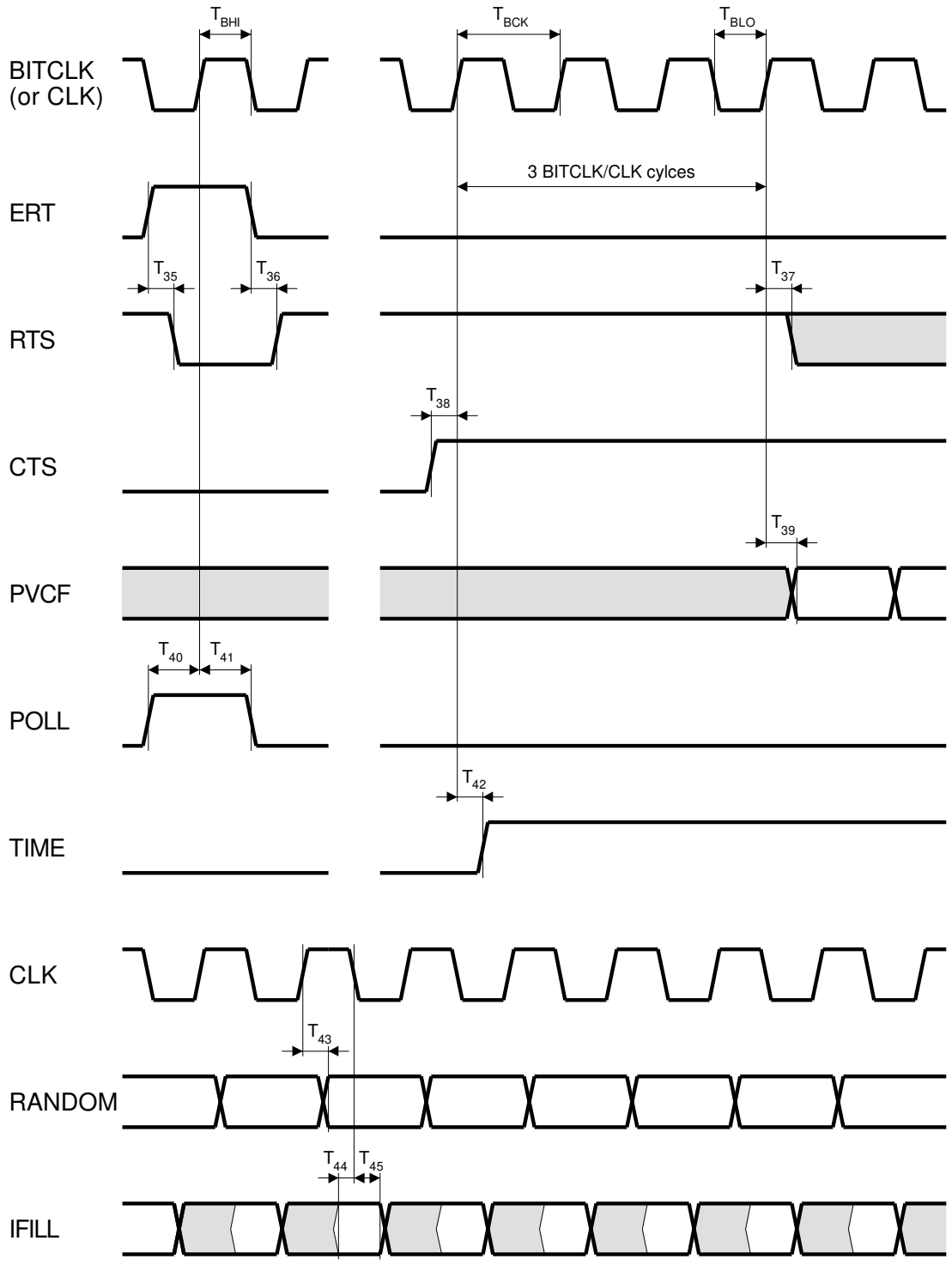

Figure 9: Timing of various signals (continued)

5.4 Mechanical data

5.4.1 Pin assignment

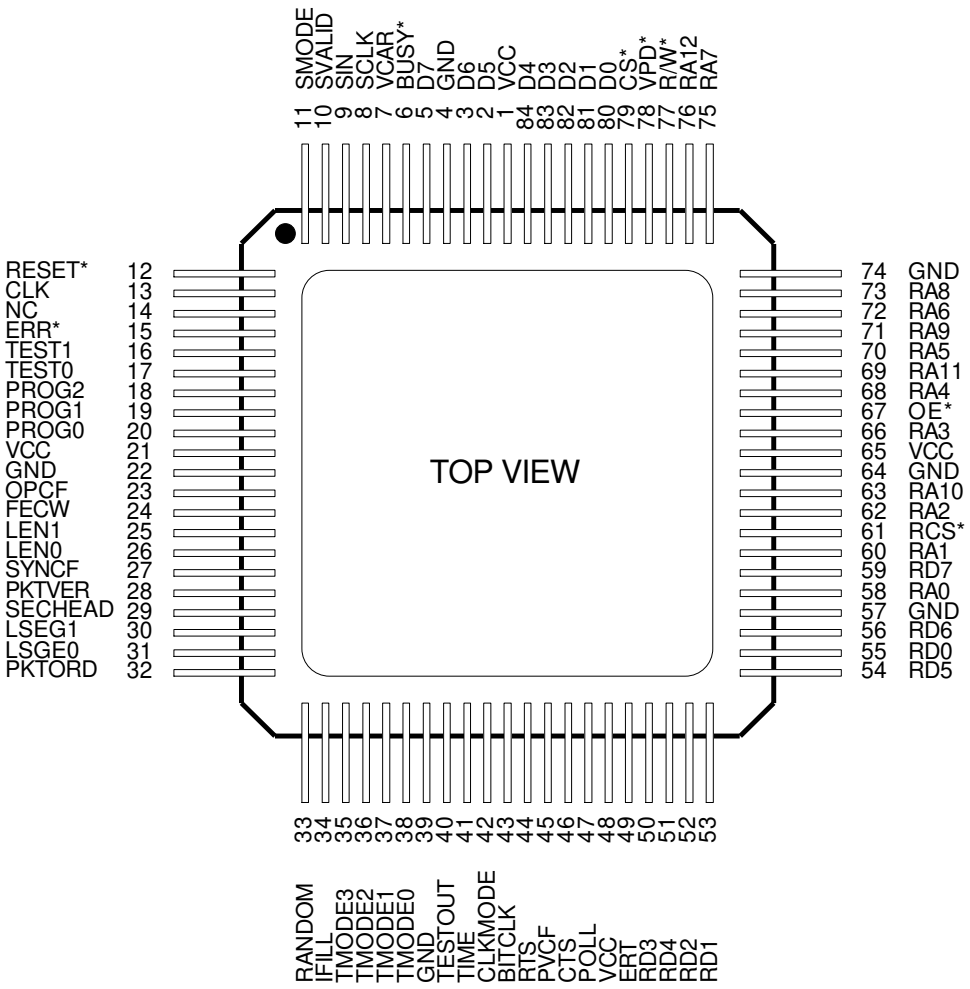

Figure 10: VCA pin assignment

5.4.2 Package dimensions

The VCA is available in an 84 pin Ceramic Quad Flat Package with 25-mil pin pitch.

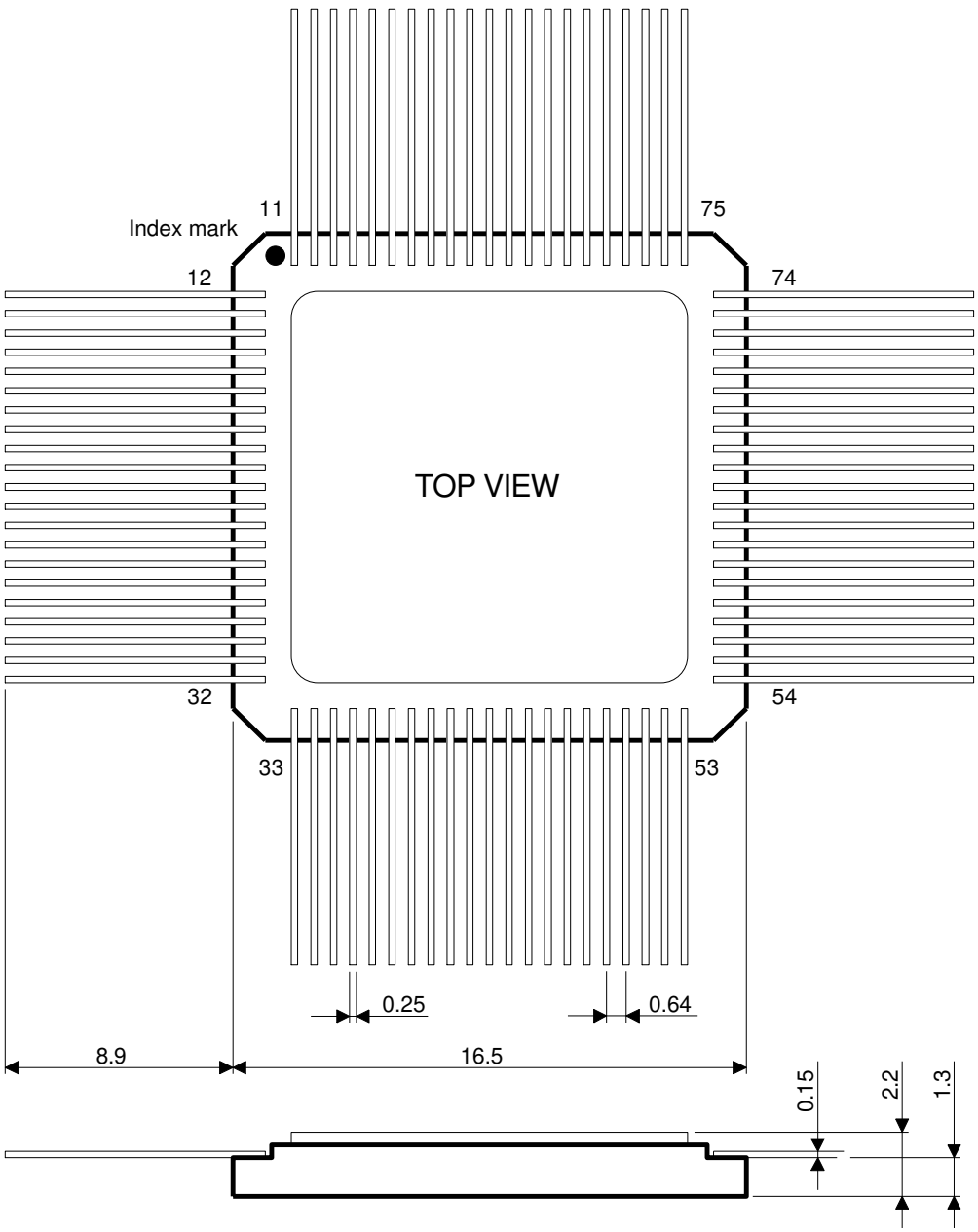

Figure 11: Dimensions for 25 mil pin pitch Ceramic Quad Flat Pack (mm)

6 ABBREVIATIONS

BIST	Built-In Self Test
CADU	Channel Access Data Unit
CCSDS	Consultative Committee for Space Data Systems
CPU	Central Processing Unit
ESA	European Space Agency
ESD	Electrostatic Discharge
FECW	Frame Error Control Word
ID	Identification
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Not Connected
OBDH	On-Board Data Handling
OPCF	Operational Control Field
PVCF	Partial Virtual Channel Frame
RAM	Random Access Memory
SEU	Single Event Upset
SOS	Silicon On Sapphire
VC	Virtual Channel
VCM	Virtual Channel Multiplexer
VCA	Virtual Channel Assembler

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